DATUM, INC., INSTRUCTION MANUAL

for

DATA LOGGER MODEL 120-131

prepared

for

LITTON INDUSTRIES

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SECTION I
INTRODUCTION

1-1 GENERAL

This manual provides the information necessary to operate and maintain the DATUM, Inc. Model 120-131 Data Logger.

1-2 PURPOSE OF EQUIPMENT

The purpose of the DATUM Model 120-131 Data Logger, hereinafter referred to as the system, is to accept analog inputs, convert these inputs into digital data and punch this converted data on a paper tape. The system also contains two up/down counters, five discrete sensors, and an elapsed time clock. The outputs of these circuits are also punched onto the paper tape. The paper tape is punched with ASCII characters.

1-3 LEADING PARTICULARS

The system consists of eight basic components:

1. Analog multiplexer
2. Analog-to-digital converter
3. Time-of-day clock
4. Control electronics
5. Up/down counter
6. Discrete sensor
7. Digital multiplexer
8. Paper tape punch

For information concerning the paper tape punch, please refer to the paper tape punch manual.

The analog multiplexer receives digital control signals from the control electronics. These signals are used to turn on a FET switch to allow an analog signal, received from the rear panel, to be connected to the input of the analog-to-digital converter. The specifications for the analog multiplexer are given in Table 1-1.

Table 1-1. Analog Multiplexer Specifications

Signal	Specifications
Full Scale Analog Input	±10V DC or Peak AC
Input Overload	±25 volts steady state ±40 volts momentary
Input Current	±50 nanoamperes maximum at 25°C, less than ±150 nanoamperes at 55°C.
Input Impedance	Same as load impedance shunted by greater than 100 megohms and less than 50 picofarads
Output Settling Time (1K source)	7.5 microseconds maximum to ±0.01% of final value

Analog-to-Digital Converter

The analog-to-digital converter is a ±10 volt instrument with a three-decimal BCD output. The specifications for the analog-to-digital converter are given in Table 1-2.

Table 1-2. ADC Specifications

Input Full Scale Range	±10 Volts DC or Peak AC
Input Resistance	100 megohms, single-ended
Digital Outputs	
Logic "1":	+4V ±1.2 Volts, .2ma max.
Logic "0":	0.4V, -6.4 ma max.
End of Conversion	Logic 1 = Data ready Logic 0 = Busy
Accuracy; including linearity, gain error, offset, and noise	±0.015% ±1/2 LSB @ 25°C
Conversion Time	26 milliseconds

Time-of-Day Clock

The time reference for the elapsed time clock and the system control electronics is derived from a 100 kHz crystal oscillator. The elapsed time clock provides four digits of information to the digital multiplexer.

Control Electronics

The control electronics receives signals from the rear panel connector (or front panel switches) and causes the system to go through the sequence required to generate the punched paper tape. The specifications for the input signals received via the rear connector panel are given in Table 1-3.

Table 1-3. Rear Panel Inputs

BNC	DESCRIPTION
CH 1	Analog input channel 1, corresponds to letter A on output tape.
CH 2	Analog input channel 2, corresponds to letter B on output tape.
CH 3	Analog input channel 3, corresponds to letter C on output tape.
CH 4	Analog input channel 4, corresponds to letter D on output tape.
	All analog input voltage ranges are ±10 volts.
UP CLOCK 1	Increase the count contained in up/down counter number 1.
DOWN CLOCK 1	Decrease the count contained in up/down counter number 1.
UP CLOCK 2	Increase the count contained in up/down counter number 2.
DOWN CLOCK 2	Decrease the count contained in up/down counter number 2.
	The clock lines to the up/down counters shall normally be at +5 volts and a pulse going to 0 volt 20 microseconds wide minimum will operate the clock.
DC 1 through DC 5	Discrete sensor inputs. These inputs normally are at 0 volt before the discrete event occurs and will go to

Table 1-3. Rear Panel Inputs (Cont'd)

BNC	DESCRIPTION
	+15 volts when the event occurs. The line must remain at +15 volts for 10 milliseconds minimum.
EXT START	This input is essentially in parallel with the start switch on the front panel. The system will enter the start mode when this signal goes from 0 volt to +5 volts. The signal must remain at +5 volts for a period of 100 microseconds minimum.
ELAPSED TIME CONTROL	This input is used to control the elapsed time counter. When the input is at 0 volt, the counter is inhibited and when the input is at +5 volts, the counter is enabled.

Up/Down Counter

The up/down counters receive up or down clock via the rear connectors and accumulate these pulses. The output of these counters is sent to the digital multiplexer. The specifications for the input signals are given in Table 1-3.

Discrete Sensor

The discrete sensors are used to monitor five external events. When the test is started and an event has not occurred, a counter will be updated every 100 milliseconds for a period of 10 seconds, or until the event occurs. At the end of the 10 seconds, the counter is recycled to

zero and the count will start again. When the event occurs, a flag is set. The flag will inhibit the counter from being updated and recycled to zero. The specifications for the input signals to the discrete sensors are given in Table I-3.

Digital Multiplexer

The digital multiplexer is used to switch the outputs of the ADC, discrete sensors, and elapsed time clock to the input of the paper tape magnet drivers at the proper time.

Table I-4. Punch Output Connector (J103) Pin Assignment

PIN	SIGNAL
1	Punch Magnets 1
2	Punch Magnets 2
3	Punch Magnets 3
4	Punch Magnets 4
5	Punch Magnets 5
6	Punch Magnets 6
7	Punch Magnets 7
8	Punch Magnets 8
9	Punch Clutch
10	-24V
11	Ground
19	Ground
20	Ground
21	Ground
22	Ground
23	Ground
24	Ground
25	Ground
26	Ground
27	Ground

SECTION II
OPERATION

2-1 INTRODUCTION

This section contains the information necessary to operate the system. The functions of all controls are explained. An operating procedure is then provided.

2-2 POWER

This switch is used to apply 115V 60Hz to the input of the system power supplies.

2-3 LEADER

This switch is used to cause the paper tape punch to feed blank tape for either leader or trailer.

2-4 RESET

When this switch is operated, the system is returned unconditionally to a standby mode.

2-5 START

This switch is used to place the system in the data logging mode. When the switch is operated, the system will commence acquiring data and punching this data on paper tape.

2-6 STOP

This switch is used to terminate the data logging operation of the system. When the switch is operated, the system will complete the scan of inputs in process and then come to a halt.

2-7 OPERATING PROCEDURE

a. The control chassis should be mounted in a 19" rack such that air flow through the chassis will not be obstructed. The paper tape punch should be mounted in a 19" rack within 4 feet of the control electronics.

b. Connect the system to 115 volts, 60 cycle, power source and connect the cable between the paper tape punch and the control chassis.

c. Connect the inputs to the system as required for the test to be performed.

d. Turn power on the system and load paper tape into the punch.

e. At this point the system is ready to start the test. This may be done one of two ways, as follows:

(1) Operate the start switch on the front panel. The system will go into the start mode and remain in the start mode until the stop or the reset switch on the front panel is operated.

(2) Allow the Ext. Start signal to go from 0 volt to +5 volts. The system will go into the start mode and remain in the start mode until the stop or reset switch on the front panel is operated.

SECTION III

THEORY OF OPERATION

3-1 INTRODUCTION

This section describes the theory of operation of the DATUM, Inc. Model 120-131 Data Logger system. A simplified block diagram is discussed first, followed by a detailed description of the logic and analog sections of the system.

When reading this section, it will be helpful for the reader to refer to the system timing diagram, Drawing Number 800442, located in Section VI of this manual.

3-2 BLOCK DIAGRAM

The system block diagram is shown in Figure 3-1.

A four-channel analog multiplexer will be used to monitor the ±10V analog inputs. The multiplexer consists of field-effect transistors, for each channel, that act as high impedance switches. Each channel is protected from damage by diode clamps. These clamp circuits allow linear operation with combined signal and common mode voltages of up to ±10 volts measured from channel to channel, or from channel to ground. The output settling time is 7.5 microseconds to ±0.01% of the output voltage step.

The output of the four-channel multiplexer is fed into an integrating analog-to-digital converter (ADC). The integrating ADC integrates the input signal over precisely one-sixtieth of a second, providing essentially infinite rejection of noise and other undesired 60 Hz signals.

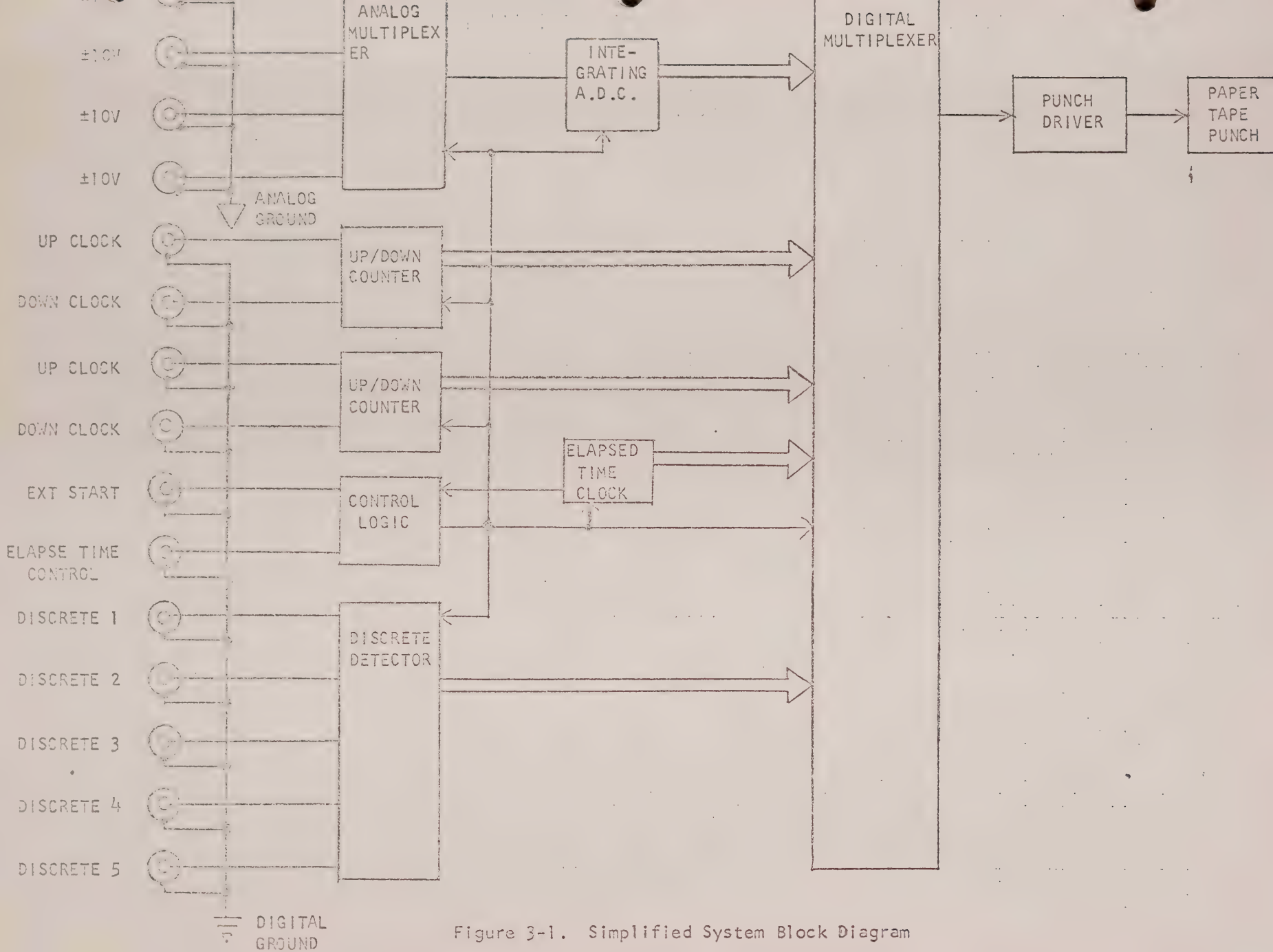


Figure 3-1. Simplified System Block Diagram

The output of the ADC is in parallel BCD words with logic levels compatible with DTL/TTL integrated circuits. The accuracy of the ADC, including linearity, gain error, offset, noise, and settling error when the input is multiplexed, is ±0.015% of full scale ±1/2 the least significant digit at 25°C. It has a stability of ±0.01% of full scale for three months.

The output of the integrating ADC is fed into one channel of a digital multiplexer. The digital multiplexer provides the switching necessary to format the paper tape sequence.

Two up/down counters are used to count the 50-microsecond pulses from the platform testing stand. These up/down counters can switch in the MHz region. The up/down counters are controlled by external up/down clocks, and reset by the control logic. The output of each counter group is fed to the digital multiplexer. The status of the up/down clock will determine the appropriate sign for each group. A plus sign is used to indicate an up count total.

An elapsed time counter, started and reset by the control logic, is also fed to the digital multiplexer.

Five separate discrete sensor circuits are employed to record the occurrence of a 0-volt to +15-volt transition. The control logic will allow and reset these sensor circuits at the proper time. The output of each circuit is fed to a separate channel of the digital multiplexer.

The control logic performs two functions: To start and stop the scan sequence; to provide the scan sequencer and subsequent paper tape formatting operation. When an external start command is received (transition from 0 to +5V), the elapsed time indicator is reset, both up/down counters are reset, and the scan process is started. Clocks are provided to the elapsed time indicator at one clock per second, the four-channel analog multiplexer is set to look at channel one, and the digital multiplexer is set to look at elapsed time. The tape format is shown in Figure 3-2.

SEC	FUNCTION	SYMBOL	NO. OF CHAR.
0	Frame Mark		3
	Time		4
	Analog Channel 1	A	5
	Analog Channel 2	B	5
	Analog Channel 3	C	5
	Analog Channel 4	D	5
1	Up/Down Counter 1	E	5
2	Up/Down Counter 2	F	5
3	Up/Down Counter 1	E	5
4	Up/Down Counter 2	F	5
5	Up/Down Counter 1	E	5
6	Up/Down Counter 2	F	5
7	Up/Down Counter 1	E	5
8	Up/Down Counter 2	F	5
9	Discrete Sensor 1	G	5
	Discrete Sensor 2	H	5
	Discrete Sensor 3	I	5
	Discrete Sensor 4	J	5
	Discrete Sensor 5	K	5

FRAME MARK: Carriage Return
Line Feed
Rub-out

TIME: Elapsed Time Tens Minutes
Unit Minutes
Tens Seconds
Unit Seconds

DISCRETE SENSOR: Symbol
Unit Seconds
Tenth Seconds
Flag
Zero

During time 0 second, the frame mark (made up of a carriage return, line feed, and rub-out characters) is recorded along with the elapsed time; also the four analog signals are multiplexed, one channel at a time, digitized and recorded on tape. During time 1 second through 8 seconds, the up/down counters are recorded on tape once every other second. The characters recorded for the analog channels and the up/down counters are: symbol, sign, most significant digit, second most significant digit, and least significant digit.

During time 9 seconds the discrete sensor outputs are recorded on the tape. The characters recorded for the discrete sensors are: symbol, unit seconds, tenth of seconds, flag (0 if discrete has not occurred, 1 if discrete has occurred), and a zero.

One scan will occur every ten seconds. Ninety-two characters per scan will be punched on the tape per scan.

3-3 LOGIC DESCRIPTION

Control Logic (Drawing Number 13296)

The switch interface logic is used to allow the operator to control the system via the front panel. When the reset switch is operated, the capacitor at X1 will be shorted out and the term POR will be true (at +5V); when the switch is released (or when power is initially applied) the POR term will remain true until the charge on the capacitor reaches the threshold of the inverter at D1. At that time, POR will be returned to a false state (0 volt).

The start switch is a momentary switch and when it is operated will set, then reset, the debounce circuit at A1, thus setting the start request flip-flop.

The stop switch is also a momentary switch. When the system is in the start mode and the stop switch is operated the debounce latch will be set. When the system completes the scan in process the term ALPHA RESET will become true; when alpha reset and the stop latch are both true, the start flip-flop will be reset and thus terminate the scanning sequence.

The leader switch is a momentary switch and will cause the tape to feed blank tape as long as the switch is held closed. When the switch is closed the latch at A1 will be set and will remain set until the switch is released.

Elapse Time Control

This input is received via the rear panel and will enable or disable the elapsed time clock. When the signal at the rear panel is open or at 0 volt the signal at A4-3 will be at 0 volt, thus inhibiting the 100 millisecond clock to the elapsed time clock at C1-10. When the signal at the rear panel is at +15 volts the signal at A4-3 will be +5 volts and will enable the clock to the elapsed time clock at C1-10.

External Start

The external start signal is received via the rear connector panel and will perform the same function as the start switch on the front panel. When the signal at the rear panel goes from 0 volt to +15 volts an integrator generates a pulse. This pulse, $\overline{ESS}$, is used to directly set the start request flip-flop.

Reset Control

This signal is derived from the scan control flip-flops and is used to reset most other flip-flops in the system to an initial state. When

the start request and the start flip-flop are reset, the term $\overline{\text{RESET}}$ will be false and reset will be true. When the start request flip-flop is set the term $\overline{\text{RESET}}$ is switched to true and reset is switched to false.

Scan Control

When the start request flip-flop is set the system reset line will be released, the CD1 and CD2 flip-flops will be reset and the start flip-flop will be enabled. When the next 1 PPS goes to 0 volt the start flip-flop will be set, which will reset the start request. The start flip-flop may be reset by either the reset or stop switch as described above.

Time Slot Counter and Decode

This counter determines which of the 1 second time intervals the system is in. The counter is disabled until the start flip-flop is set and the counter will be jam reset to zero at the end of the 10-second scan.

Clock Control

This circuit is used to generate the 10 PPS to the elapsed time clock and to generate the 1 PPS used on the control card.

Clock Dividers

The clock dividers CD1 and CD2 are used to divide the 100 Hz signal from the elapsed time card down to 25 Hz. The 25 Hz is then used as the basic frequency of the punch.

Sequence Control Logic

This logic is the basic programer for the system. It determines what data will be gated to the punch driver. The PCENA flip-flop will be turned on at the beginning of each 1 second interval of the scan and will remain on until all data for that interval has been punched. The PCRST flip-flop is used to reset the PCENA; therefore, PCRST detects when the data for any given 1 second interval is punched. During time 0 second and 9 seconds, the PCENA will remain set for the entire 1 second period.

PCCHAR is used to determine which character of a word will be gated to the punch drivers. When the PCENA is set, the PCCHAR is enabled and will be reset by the next 10 microsecond pulse. With PCCHAR set, the reset to the divide-by-10 BCD counter at H2 is released and the clock to the counter is decoded at H3. The output of the decoder is used to reset the PCCHAR.

The counter composed of ACTR1, ACTR2, ACTR4, and ACTR8 is used to determine which word will be gated to the punch drivers. This counter is a divide-by-12 binary counter, but it is modified to ping-pong between 5 and 6 when the SPCT flip-flop is set. The PCCHAR is used as the clock to the ACTR. The output of the counter is decoded by 4-to-10-line decodes at J2 and J3. When the output of the decoder is 3 the SPCT flip-flop is set. This will occur during time 0 second of a scan. The SPCT flip-flop will remain set until time 7 seconds, when it is reset.

The ACTR is then allowed to reach a count of 11, where the ALPHA RESET flip-flop is set. When ALPHA RESET is set, the ACTR is directly reset to zero and the cycle begins again.

Multiplexer Control

This logic is used to control the analog multiplexer and the analog-to-digital converter. The MUX ENA flip-flop will be set during

time 0 second when the PCCHAR flip-flop is turned off after punching the frame mark and time word. With MUX ENA on the digitize will be generated by character 0 and CD1 and $\overline{CD2}$. The clock to the ADDCTR (multiplexer address counter) will be generated by character 1. MUX ENA will be reset during time 1 when the PCCHAR is turned off.

Punch Clock Control

This logic is used to gate data to the punch drivers and to provide the signal to the punch clutch. The gate at J1-2 is used in conjunction with the leader switch to generate the punch clutch signal. The gate at B2-11 is used to generate the punch clutch signal when data is being punched. The circuitry associated with the gate at A4-13 is a one-shot with a variable time delay between 11 and 20 milliseconds.

Format Logic

This logic is used to gate the most significant four bits of data to the punch drivers. This logic also provides the enable terms which gate the least significant four bits of data from the ADC and the up/down counters to the punch driver.

Up/Down Counter Logic (Drawing 13284)

The up/down counters contain all the electronics required to accumulate the up or down clocks, transfer the output of the accumulator to a storage register, and multiplex the output of the storage register into four words, four bits per word, to be sent to the system digital multiplexer.

The up clock and down clock are received on pins 45 and 46 respectively and are OR'ed together at B4-2. When a clock is received, B4-2 will

go from +5 volts to 0 volt. This will cause the circuits of D4-14, B4-13 and E2-5, E4-2 to generate a pulse. The pulse generated by E2-5 and E4-3 is used to clock the accumulator. The pulse generated by D4-14 and B4-13 is used to prevent the XFER flip-flop from transferring the accumulator into the storage register until the clock has been completed by the accumulator.

The XFER flip-flop, as implied above, is used to transfer the contents of the accumulator into the storage register. This is done each 1 second by the 1 PPS.

The up flip-flop is used along with the sign flip-flop to determine whether the clock will cause the counter to increase or decrease its count. Assume the accumulator has a count of -190 and an up clock is received. The accumulator will go to a count of -189. The logic on the right side of sheet 2 shows the logic for detecting zero, the sign bit, and the increase/decrease decoding.

Drawing 13284, Sheet 3

The least significant decade of the up/down counter is shown across the top of sheet 3. This counter is made up of three decades which are identical except that the third decade does not have a carry output. The output code of the up/down counter is the commonly used BCD (8-4-2-1) code, and the output sequence generated is the binary equivalent of the decimal numbers 0 through 9. The second and third decades are shown on sheet 4.

The storage register is shown on the bottom left side of sheet 3. This register is made up of three four-bit storage elements and a flip-flop. The output multiplexer for the up/down counter is shown on the right side of sheet 3.

Discrete Detector (Drawing 13294, Sheet 2)

The discrete detector logic receives an input via the rear connector panel to indicate the occurrence of an external event. When the event occurs the discrete detector logic will remember the time, and set a flag. The flag and the time (to the nearest tenth of a second), along with an identification symbol, will be punched onto the paper tape during time 9 seconds. There are five independent discrete circuits on the discrete detector card.

When the scan is started the discrete flag (flag 1), the discrete detector (DISC1), and the counter at K1 and K2 will be reset. Therefore, the clock to K1-8 is a function of the 100 millisecond input at pin 12. The counter at K1 and K2 will count to 9.9 seconds then recycle to 0.0 second until DISC1 becomes set. When DISC1 is set the clock to K1-8 will be inhibited via K3-4 and the counter will remain at the same number. The flag may be set at time 9 seconds only; this will prevent the data to the punch from changing during a punch cycle. The flag will be set at time 9 seconds only if the discrete has occurred prior to that time.

Discrete Detector (Drawing 13294, Sheet 3)

This sheet shows all the gates necessary to multiplex the output of the discrete detectors into 5 words, 3 characters per word, four bits per charactor. Alpha 7 is the first word and the three characters are gated onto the output lines by TCF1, TCF2, and TCF3.

Punch Driver (Drawing 13295)

This card contains 10 identical circuits. Nine of these circuits are used to drive the paper tape punch magnets.

The input to the circuit is normally at +5 volts or open. The input being at +5V will bias the base of the first transistor at approximately +2 volts and turn the transistor off. With the first transistor off, the base of the second transistor will be at +5 volts and thus biased off.

When the input to the circuit is switched to 0 volt, the base of the first transistor goes toward -2 volts and turns the first transistor on. With the first transistor on the base of the second transistor is pulled toward a -2 volts. As the base of the second transistor goes to -.5 volt, it will turn on and clamp the base of the second transistor at -.5 volt. The diode on the collector of the transistors is used to suppress the fly-back voltage spike caused by the coil when the driver is turned off.

Time-of-Day Clock

The Time-of-Day Clock is a digital clock with DTL/TTL outputs corresponding to seconds, minutes, and hours. The clock may be controlled by an internal 100 kHz crystal controlled oscillator or by an external 60 Hz standard. The Time-of-Day Clock card also contains an intervalometer.

Each gate of the crystal oscillator circuits is made to operate in a linear condition by the negative feedback resistors. The resulting amplifiers have a gain of about 10. The coupling capacitor connects the amplifiers in cascade. The second amplifier drives the crystal, causing a current of crystal frequency to pass through the feedback capacitor to the input of the first amplifier, forming a positive feedback loop. Any disturbance in the loop, like applying power, will cause oscillations at the crystal frequency.

The output of the oscillator is applied to a divide-by-10,000 BCD counter (NM01-NM16) such that the output of the counter (NM16) is 10 PPS.

If the clock is to use the 100 kHz as the time base, then the output of the BCD counter is connected to a divide-by-10 BCD counter (NM17-NM20). The output of this divide-by-10 counter (NM20) is a 1 PPS and is used to update the clock counter/registers.

The unit seconds counter is a BCD divide-by-10 counter (NC01-NC04). The unit seconds 8 bit is used to clock the tens second counter (NC05-NC07). The tens of seconds counter is a divide-by-6 counter. When the counter reaches a count of 6, a pulse approximately 1 microsecond wide is applied to the reset of the tens of seconds counter chip and thus resets the counter to "0." This 1 microsecond pulse is also used to clock the input to the unit minutes counter. The unit minutes and tens of minutes counters operate the same as the unit seconds and the tens of seconds counters.

The hours counter is a BCD divide-by-24 and is made up of a BCD divide-by-10 and a divide-by-3. When this counter reaches a count of 24 a 1 microsecond pulse is formed by the gate C4, C2, and C1. This 1 microsecond pulse is used to reset the hours counter to "0."

When a ground is applied to pin 18 the counter NM17-NM20 will be held in the reset state and the clock will be in the hold mode.

The clock is preset by applying the BCD digit to pins 4, 9, 7, and 11, then applying a ground to the preset pin of the proper decade. Pins 4, 9, 7, and 11 are the BCD digit and are connected to all the clock counters in parallel. The preset line for each counter decade is a unique pin.

The intervalometer may be selected to divide by 1, 2, or 3. The input to the intervalometer may be selected to be 1 second, 10 seconds, 1 minute, 10 minutes, or 1 hour. Therefore, the output of the intervalometer may be any combination of the input and the divider, i.e., 1 second, 2 seconds, 3 seconds, 10 seconds, 20 seconds, 30 seconds, etc.

Digital Multiplexer (Drawing 13293)

The digital multiplexer is basically an 8 input by 4 output digital matrix, made up of 2 input NAND gates. One input of the NAND gate is a data input, and the second input of the gate is the enabling term. The enabling term is driven from a 2 input NOR gate, whose inputs are brought out to connector pins and may be programed as required. When the 2 inputs to the enabling gate are at 0 volt that multiplexer term will be enabled.

The output of the multiplexers are dot OR'ed. The multiplexer may be expanded by connecting the outputs of another similar multiplexer in parallel.

There are two of these digital multiplexers used in the data logger system. The first multiplexer, located in card slot J20, is used to gate the frame mark and time information to the punch drivers. The second multiplexer, located in card slot J21, is used to gate the output of the alpha counter, the ADC, the up/down counters, and the discrete detectors to the punch drivers.

Integrating Analog-to-Digital Converter

The integrating analog-to-digital converter digitizes bipolar inputs of 0 to ±10 volts full scale into readings of four decimal digits and polarity sign. Input signals are digitized over precisely one-sixtieth of a second, providing essentially infinite rejection of noise and other undesired 60 Hz signals. Digital outputs are parallel words in BCD (8-4-2-1) format, with logic levels compatible with DTL/TTL integrated circuits.

The converter consists of two cards; the analog card contains the input buffer amplifier, precision dc reference standard, high accuracy

converter network, and integrating amplifier. The logic card contains the digital logic circuits.

A standard feature of the integrating ADC is an output storage register which holds the preceding reading at the output during the conversion process. This means that additional data storage to provide a non-blinking visual readout or to couple to digital printers, paper tape punches, or magnetic tape recorders is not required.

Circuit Operation

The logic is operated synchronously with a 1.2 MC clock generated by gate E4, and regulated by a 1.2 Mz crystal. The clock is referred to schematically as DCCL.

The conversion is initiated by a positive pulse on the digitize line. The pulse causes FC01 to go high, which in turn causes the EOC output to go low. The EOC output stays low during the conversion process indicating that the ADC is converting, after which the EOC output will return high. FC01 also resets the ripple counter consisting of B3, B5, B4, and B2.

The first clock pulse that comes after the digitize pulse sets FC01 low and FC02 high. FC02 enables the clock into the ripple counter and the count begins accumulating. Simultaneously, FC02 gates the input switch driver Q25, on the analog board. Q25, Q18, and Q19 are ultra high speed switching transistors which turn on the FET input switch made up of Q1 and Q2. The input signal goes through the unity gain, high input impedance buffer amplifier, A1, and is integrated by the integrating amplifier made up of A2, C6, and R7. The zero control, R13, sums current into the integrator summing junction to allow a zero output indication for inputs

of up to .5% FS. The integration process begins with Q1 and Q2 being turned on. The gain of the integrator has been chosen so that a full scale input will provide maximum resolution without ever driving the amplifier. As the integrator output moves from zero, the μa 710 comparator output switches in that direction. The μa 710 output is detected by the differential switch Q10, Q11 and is coupled to the comparator input on the logic card through FET switch Q12, Q13. An FET switch was chosen to minimize the current flowing between the analog and digital domains. The comparator output (input on logic card) is high for negative inputs and low for positive. This level sets FC03 properly so that the correct reference switch turns on. The integrator continues until the counter reaches 20,000 (1/60 second), then NC19 goes high. At this time $\overline{NC19}$ gates off the input switch and NC19 gates on the reference switch opposite in sign to the input, causing the integrator to integrate back to 0 volt. The reference voltages are created by using a highly stable zener diode to reference an I.C. amplifier and using a second I.C. amplifier as an inverter. A pot, R58, is provided to adjust the gain balance and R66 to adjust the gain. The references, like the input, are switched through ultra high speed transistors and a pair of FET's. When the integrator output has crossed through 0 volt, the μa 710 output will make a step change in voltage. This step is seen at the comparator output and causes FC02 to go low.

FC02 disables the clock to stop the count and resets the integrator to zero. The value left in the counter is proportional to the dc input voltage during the integrate time. $\overline{FC02}$ enables the data to be transferred to the output storage register to display the count at the output. The count remains available at the output until after a new conversion has been accomplished.

SECTION IV

MAINTENANCE

4.1 LOGIC ELEMENTS

All logic elements are Signetics TTL or Utilogic integrated circuits in dual-inline packages. Logic diagrams for these elements can be found at the back of this section.

The logic elements are mounted in wire-wrap sockets on printed circuit cards. All circuit interconnections are made by wire-wrap connections. Circuit elements are easily replaceable by removing from their sockets and replacing with an equivalent element.

Integrated circuits are used throughout wherever possible. Exceptions are relay and lamp drivers.

4.2 Logic Symbols

The logic symbols are derived from MIL STD 806B and are utilized in such a manner that signals can be traced through the logic in terms of "High" and "Low" (+2.5 to +5V) and (0V) by examination of the logic symbols without the need to memorize the electrical characteristics (NAND, NOR, AND, OR, etc.) of the circuits (which most other logic drawing schemes require).

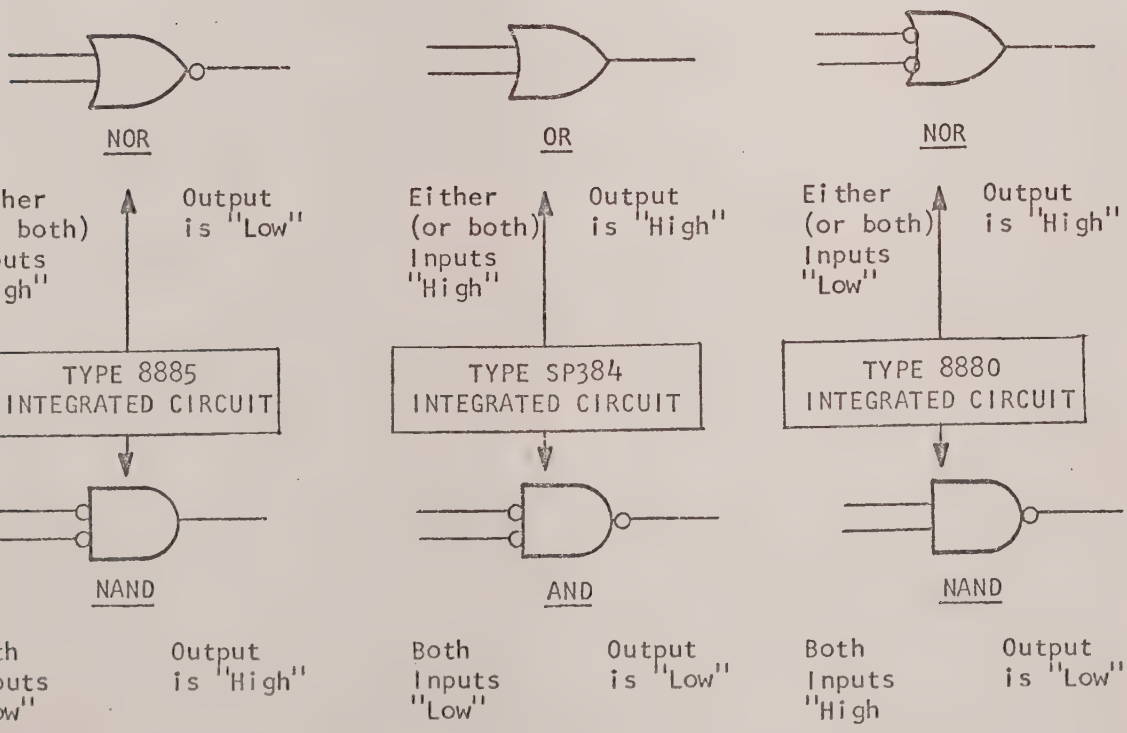
The "High" and "Low" signal level indication is illustrated by a straight line for a "high" signal and a small circle for a "low" signal level. The following symbol shapes are used:

"OR"
SYMBOL

"AND"
SYMBOL

The use of straight lines or circles at inputs and outputs of these basic symbols completely defines the function the circuit performs, the input signal levels required to activate the circuit, and the output signal level when the circuit is activated.

Some examples follow:

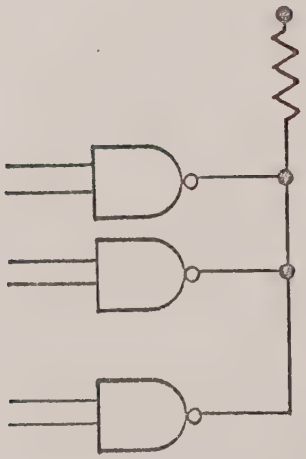


Note that the Type 8885 integrated circuit can be used as a "high" input NOR or a "low" input NAND.

Note also that the Type 8880 integrated circuit can be used as a "low" input NOR or a "high" input NAND.

Note that the Type SP 384 integrated circuit can be used as a "high" input OR or a "low" input AND.

A "low wired OR" or a "high wired AND" function can also be implemented with certain integrated circuits by tying the outputs together and adding an external discrete resistor "pull up."



+5

"Pull Up" Resistor

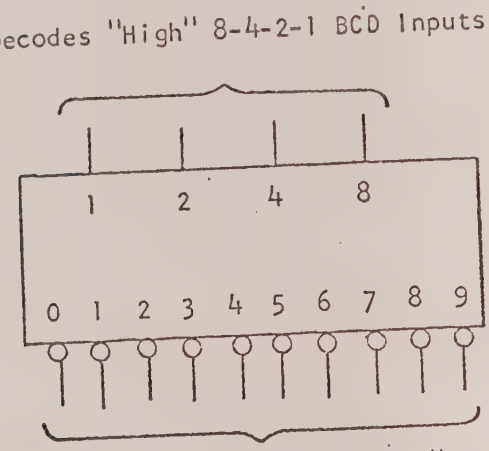
1. <u>"Low Wired OR"</u>

   (Any NAND gate output goes "low" the bus goes "low.")

2. <u>"High Wired AND"</u>

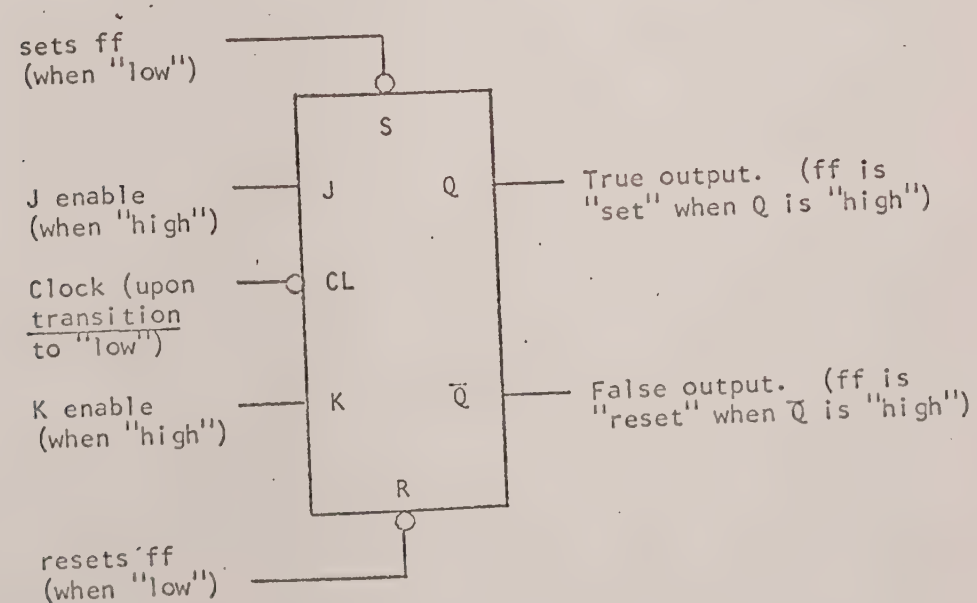
   <u>All</u> NAND gate outputs must be "high" in order for the bus to be "high."

The 4-to-10-line decoder symbol is:



"4-TO-10-LINE DECODER" SYMBOL

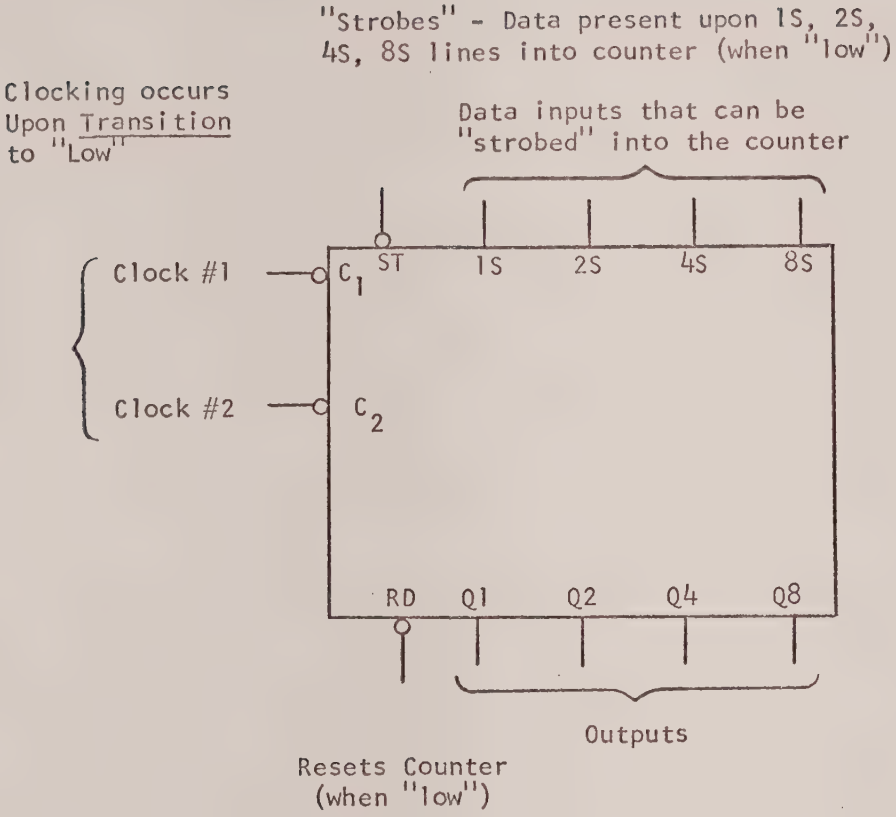
The J-K flip-flop symbol is:



J-K FLIP-FLOP TRUTH TABLE

Input Levels Before Clock		F.F. State After Clock
J	K	
Low	Low	Same as Before Clock
Low	High	Reset
High	Low	Set
High	High	Opposite of Before Clock

As illustrated in the Truth Table, the J-K flip-flop has no "forbidden" combination for its J and K inputs. If both inputs are enabled, the clock merely causes the flip-flop to toggle to the opposite state.



Note that the clocking action takes place upon the transition of the clocks from the "high" level to the "low" level while the strobe and reset functions are active all the time the strobe or reset signal is at the "low" level.

Clock #1 (C1) toggles the first flip-flop (Q1) in the counter. Flip-flop Q1 is a divide-by-2. Clock #2 (C2) clocks the next three flip-flops (Q2, Q4, Q8) in a divide-by-5 configuration. Connecting Q1 output to clock #2 provides a 1-2-4-8 BCD coded divide-by-10 configuration.

This circuit is also used quite regularly as a four-bit storage register, particularly in cases where a data display register is required.

4.3 How to Use Drawings

The drawings consist of:

a) Top Assembly Card Location Chart.
b) Block Diagram.
c) Detailed Logic Diagrams.
d) Schematics.
e) Card Assembly Drawings.
f) Integrated Circuit Schematics.

The Top Assembly Drawing/Card location chart shows pertinent mechanical details and the card slot versus card assembly number.

The Block Diagram illustrates the system in simplified form and carries card location numbers which correspond to the location within the cage that the logic block appears.

The Detailed Logic Diagrams carry the same drawing number as the card on which they appear.

The physical location of each circuit is illustrated on the Logic Diagrams by card slot number and chip location on the card. The chip location designation corresponds to the column (A-N) and row (1-4) in which the I.C. chip is located on the board.

The assembly drawing number is the same number that is stamped on the circuit card (or may be found by card slot number on the top assembly/card location chart drawing).

Circuit outputs are given mnemonic terms for "memory tickling".

Input signals carry these mnemonic terms and also a "dash" number if the origin of the signal is on a different sheet of logic drawings. The "dash" number refers to the "sheet" number on which the signal originates.

The "X" numbers by discrete components give the physical location of the discrete component on the board. There are X1 through X21 locations for discrete components on each logic board.

Test points are indicated by circled numbers.

Schematics are included for discrete circuit cards and/or DATUM universal "matrix" cards which have discrete circuitry not completely specified in the Detailed Logic Diagrams. The schematics carry the assembly number of the circuit board as the drawing number (for easy correlation).

The card assembly drawings carry the same number as the circuit card assembly and illustrate the chip types by manufacturer's part number. This is necessary because the detailed logics merely illustrate the physical location of the chip and not the chip type.

The integrated circuit schematics are organized by manufacturer's part number and illustrate power pins for each chip as well as all input/output pins.

If any further information is required about the integrated circuits, it is recommended that the DCL Series 8000 and the Utilogic II designer's handbooks be acquired from the Signetics Corporation, 811 East Arques Avenue, Sunnyvale, California 94086.

SECTION V

POWER SUPPLY

5-1 General

This power supply is a rack-mounted unit to be used in our standard small systems. It has the capability of handling one module of logic in most systems and allows for a compact, self-powered unit needing no external voltages for most applications.

5-2 Power Supply (See Drawing 800,015, 4 sheets, 940,001, 2 sheets, and 76014)

As may be seen from the block diagram (Figures 1, 2, and 3), the power supply consists of an isolation transformer, rectifier/filter, and a series dissipative regulator for the regulated outputs. The +5V, 4.5A output has overvoltage protection (crowbar) in the form of an SCR across the output and a fuse in the return line. All the regulated outputs have overcurrent protection of a nature sufficient to protect the power supply under short circuit conditions. The current limit will also protect the power supply under overload conditions for a limited period of time.

The unit is designed to operate at rated output in a 70°C natural convection ambient.

The transformer primary is split to allow operation at 115V ac nominal or 230V ac nominal. The units are supplied with the primaries connected in parallel for 115V ac operation. The primaries must be reconnected in series for 230V ac operation. The ac line fuse is 1.25A, 125V, 3AG, Slo Blo.

The +230V unregulated output is designed to have a ripple voltage of approximately 5V peak-to-peak at 120 Hz. The bleeder resistors are designed to reduce the output voltage to a safe level in approximately five seconds under no-load conditions. This potentially dangerous voltage and its relatively slow decay time must be avoided with care when adjusting or troubleshooting the power supply.

The +24V output is fullwave rectified, unfiltered, unregulated for driving lamps.

The +5V regulator operates as indicated by the block diagram (Figure 1) and Schematic Diagram 800,015, sheet 2. Drive current is supplied to pass transistor Q23 through R30 and Q22. The drive current to Q22 is limited by shunting drive current through Q21. Transistor Q21 is driven by voltage reference amplifier Q24 or current reference amplifier Q20, depending on the mode of operation. During normal operation, the proper drive current level is determined by comparing the voltage across reference diode CR24 to the voltage across divider resistor R36 and compensation diodes CR27 and CR28. Thus, if the output voltage is high, Q24 is driven on, turning Q21 on. When Q21 is turned on, Q22 and Q23 are turned off, which decreases the output voltage. The voltage across CR24 should be approximately 6.8 volts and the voltage across R36, CR27 and CR28 should be approximately 7.4 volts for normal operation. Under overload conditions, the voltage developed across R25 and R26 overcomes the bias provided by divider R27, R32 and R34 driving Q20 on and turning Q23 off. Under normal operating conditions, the base emitter of Q20 will be forward biased approximately 0.3V. The divider network will be set at the factory to initiate current limit at approximately 6A output current. At this current level the base emitter of Q20 will be forward biased approximately 0.5V. Reference bias voltage for the +5V regulator is taken from the +34V unregulated supply. This voltage is regulated by a two-stage zener regulator CR23, CR24 and CR25 as shown by the Schematic Diagram. The +5V output has overvoltage protection provided by silicon controlled rectifier CR26 and fuse F2. Voltage reference for the

crowbar is provided by reference diode CR25 and divider resistors R40 and R41. The divider will be set at the factory to turn Q25 on at an output voltage between 5.8V and 6.5V. When Q25 is on, silicon controlled rectifier CR26 is fired, reducing theoutput voltage to approximately 1.25V. If the regulator has been disabled, the fuse F2 will open, disconnecting the power supply from the load. F2 is a standard 6A, 32V, 3AG fuse.

The "analog" supplies (±15 and ±20) operate as indicated by the Block Diagram (Figures 2 and 3) and Schematic Diagram 800,015, sheets 3 and 4. Both positive voltage regulators are supplied unregulated voltage from the same rectifier-filter as are both negative voltage regulators. This allows any load between 0.05A and 0.25A to be supplied by either the 15V or 20V supply with a 0.30A maximum total output per positive or negative pair.

The -20V transistor Q51 is driven from the constant current source Q53 through Q52. Control is achieved by shunting the drive current through voltage reference amplifier Q54 or current reference amplifier Q55. Under normal operating conditions, the proper drive current level is determined by comparing the voltage across reference diode CR54 to the voltage across divider resistor R65. When the output voltage is high, Q54 is turned on, reducing the frive current to Q52 and turning Q51 off, thus reducing the output voltage. For normal operations the reference voltage should be approximately 6.2V and the voltage across R65 should be approximately 6.8V. Under normal conditions the base-emitter junction of Q55 should be forward biased at approximately 0.3V or less as determined by divider R53, R60 and R59. When the output current reaches a level (0.30A to 0.35A) sufficient to override the factory preset bias, Q55 will turn on, reducing the drive current to Q52 and turning Q51 off. Under overload conditions the base-emitter of Q55 will be forward biased approximately 0.5V.

The +15V regulator operates in a manner identical to the +20V regulator.

The -15V pass transistor is direct driven through R91. Control is achieved by shunting drive current through Q92. Under normal operating conditions, the proper drive current level is determined by comparing the voltage developed across divider resistor R107 to the reference diode voltage CR94. When the output is high, Q95 is driven on. This increases current through Q91 turning on and reducing drive to Q93. This turns Q93 off, thereby reducing the output voltage. For normal operation, the reference voltage should be approximately 6.2V and the voltage across R107 should be approximately 6.8V. At rated or less output current, the base-emitter junction of current reference amplifier Q94 will be forward biased approximately 0.2V. When the output current approaches the limit value preset at the factory (0.3 to 0.35A), the voltage across R98 will override the bias provided by R97, R94 and R96, turning Q94 on, which turns Q92 on, reducing drive to Q93 and turning it off. Under overload conditions, the base emitter junction of Q93 will be forward biased approximately 0.5V.

The -20V regulator operates in a manner identical to the -15V regulator.

VOLTAGE AND CURRENT LIMIT ADJUSTMENTS

		Variable or Selected Component		
Output	Voltage Adjust	Voltage Range	Current Limit	Over Voltage Limit
+5	R37 (Variable)	R38	R31	R40
+20	R62 (Variable	R63	R58	-
+15	R82 (Variable)	R83	R78	-
-15	R104 (Variable)	R105	R95	-
-20	R124 (Variable)	R125	R115	-

CAUTION

Wiper of variable resistor used for output voltage adjust is electrically connected to the resistor case. Shorting to an electrical conductor may result in damage to the regulator.

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TROUBLESHOOTING INSTRUCTIONS

	Type of Failure	Probable Cause	Corrective Action
1.	All output voltages at zero.	Input fuse blown.	Replace with 1.25A, 125V 3AG Slo-Blo fuse.
		Transformer primary open.	Check for continuity.
2.	No voltage at transformer secondary.	Open secondary return.	Check for continuity.
3.	Unregulated voltage less than rated output plus 20V (at minimum input voltage).	Low input voltage or overloaded output.	Check line voltage and overloaded outputs.
		Open winding or diode on one side of secondary.	Check for continuity.
4.	No output voltage.	Open pass transistor.	Check for positive base voltage (0.6V).
		Regulator in current limit.	Check for overload or low set point by reducing load. Check for shorted current limit transistor.
		Output fuse blown.	See below.
5.	Output not regulated.	Defective reference diode.	Check for proper reference voltage.
		Defective transistor.	Check for shorted or open transistor.
		Defective variable resistor.	Check by attempting to adjust voltage. Check continuity of divider circuit.

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TROUBLESHOOTING INSTRUCTIONS
(continued)

	Type of Failure	Probable Cause	Corrective Action
6.	Output fuse open +5V only.	Overload.	Reduce load to rated level. Replacement fuse 6A, 32V, 3AG, Standard.
		Shorted pass transistor.	Replace.
		Overvoltage protection activated with defective current limit.	Check for shorted pass transistor or open current limit transistor.
7.	+5V output reduced to 1.25V.	Overvoltage protection activated without regulator failure.	Remove input voltage to allow SCR to turn off.
8.	Excessive 120 Hz ripple (+5V output).	Defective 12V reference.	Check for proper reference voltage.
9.	Overvoltage protection activated at less than 5.7V or more than 6.3V (+5V output).	Defective reference.	Check for proper reference voltage.
		Shorted or open transistor.	Check continuity.
		Improperly adjusted.	Reset by selecting R40.

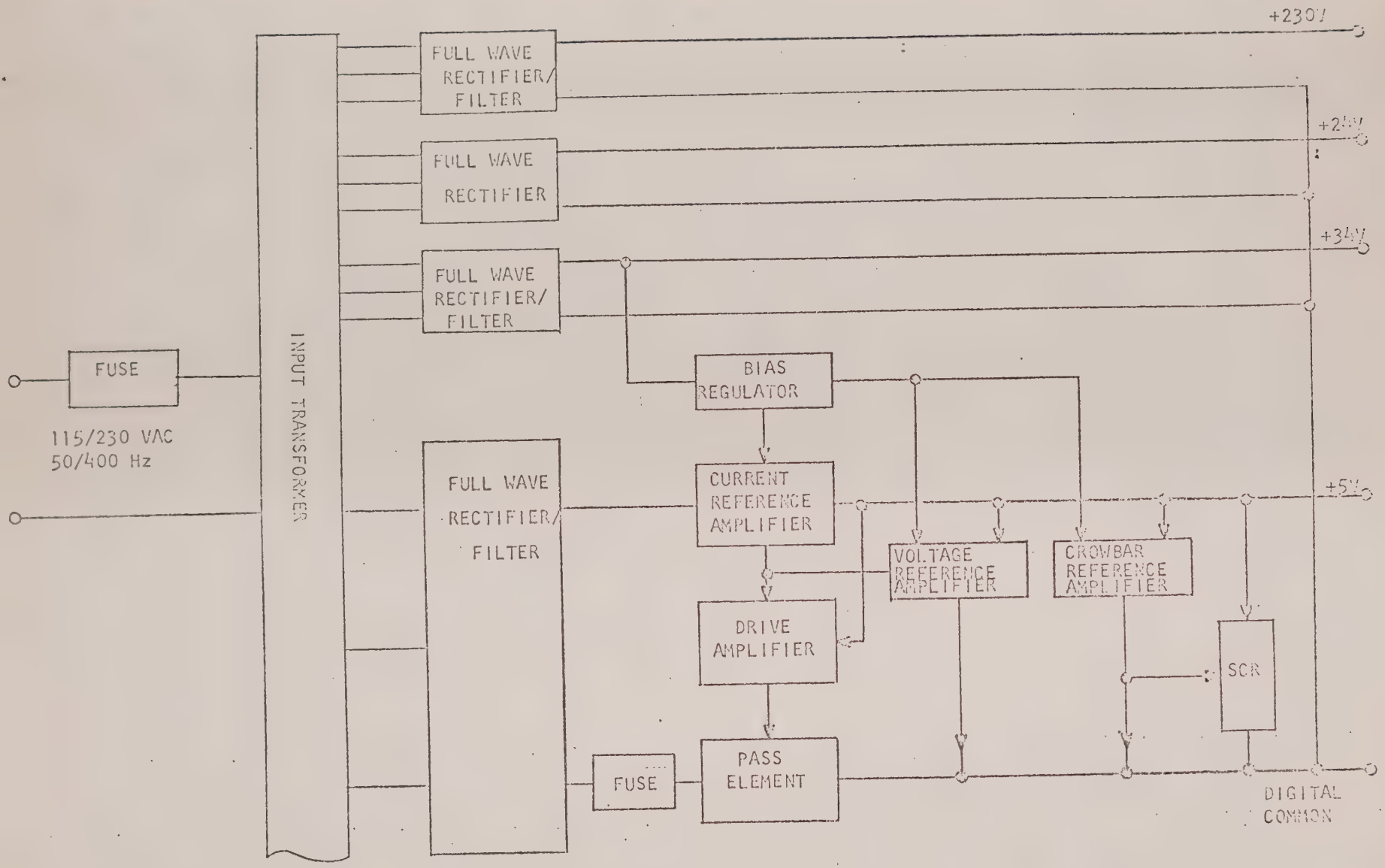


Figure 1. Digital Power Supply Block Diagram

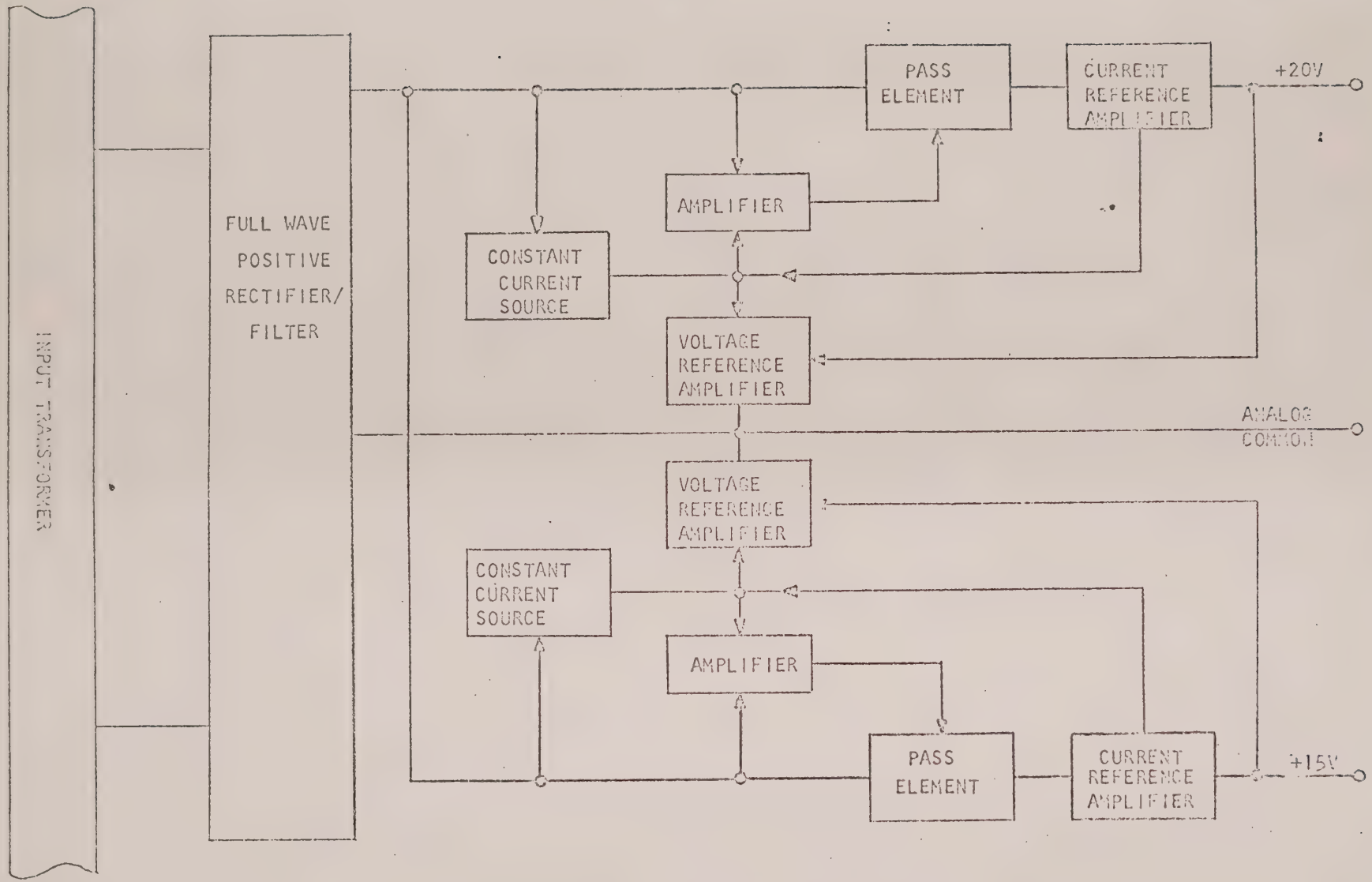


Figure 2. Analog Supply Positive Voltage Regulator Block Diagram

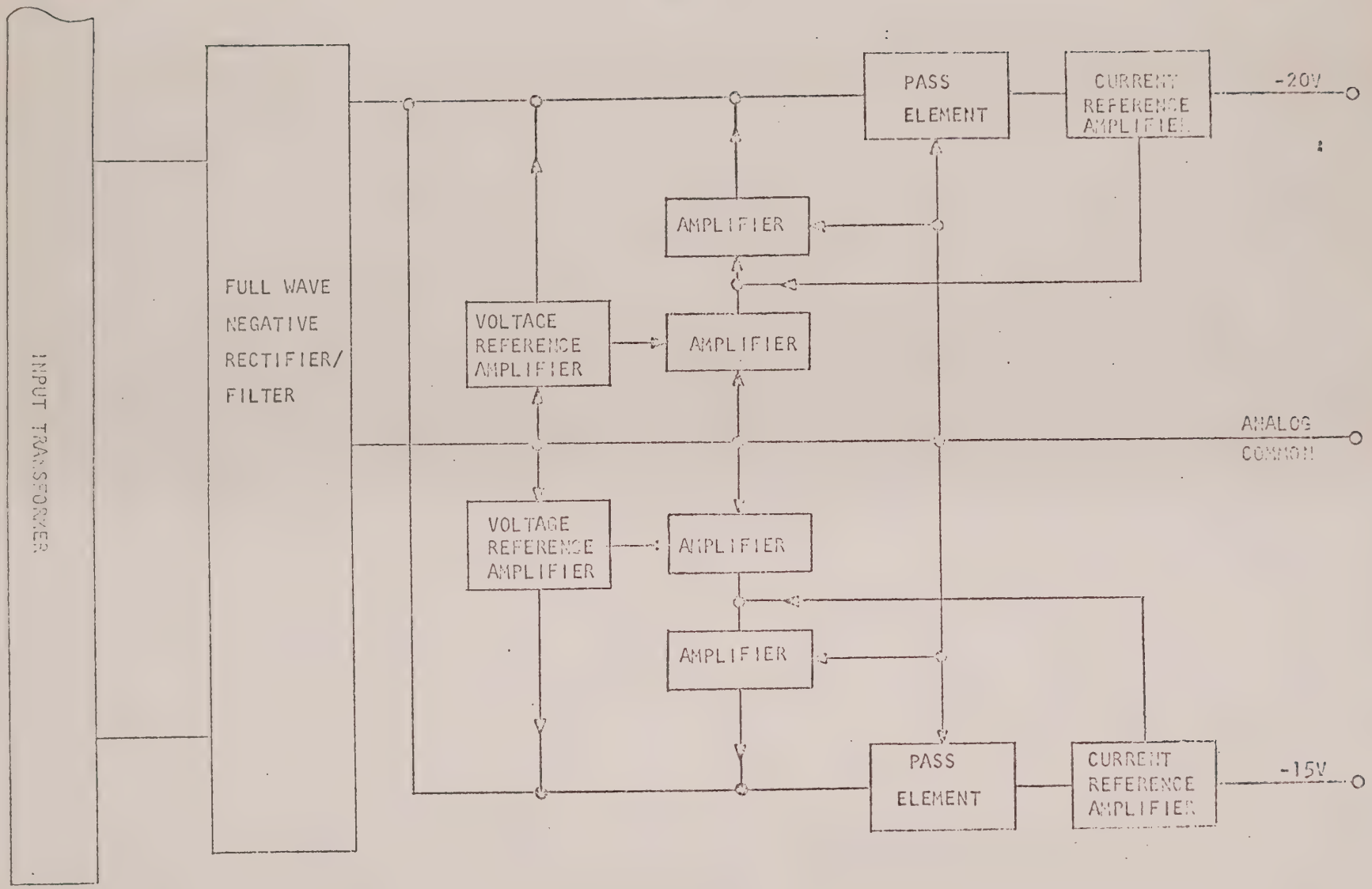
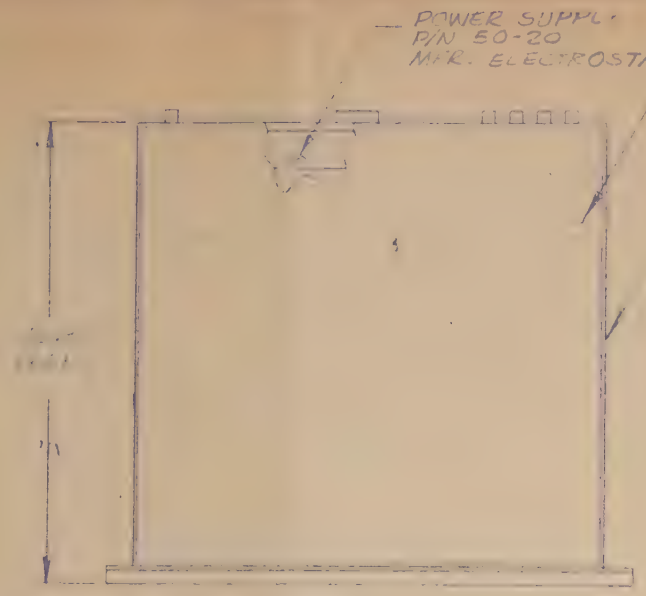


Figure 3. Analog Supply, Negative Voltage Regulator

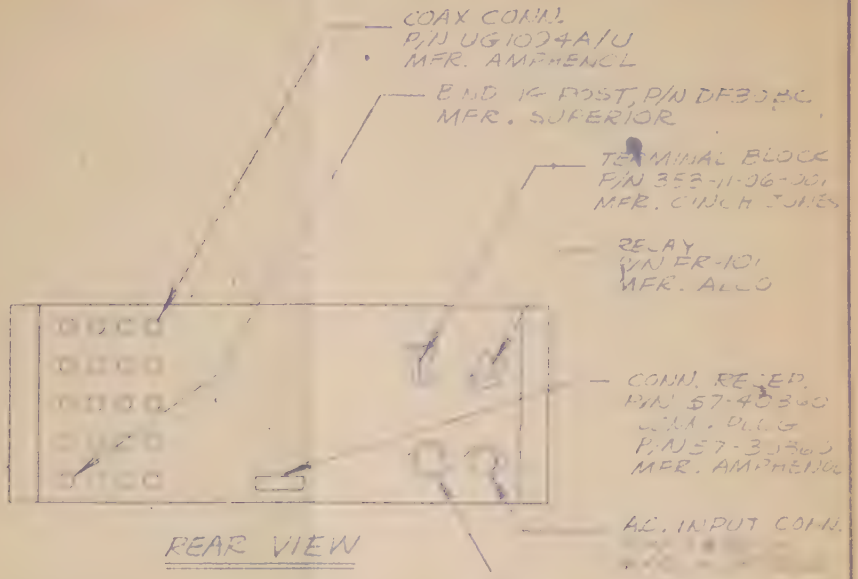
LIST OF DRAWINGS

120-131	Top Assembly
12006	Analog Multiplexer
12108	Integrating ADC
13283	Integrating ADC Logic
13284	Up/Down Counter
13294	Discrete Detector
13295	-24V Solenoid Driver
13296	Control Logic
13285	TOD Clock
13293	Digital Multiplexer
800015	Power Supply
800442	System Timing Diagram
940001	Power Supply

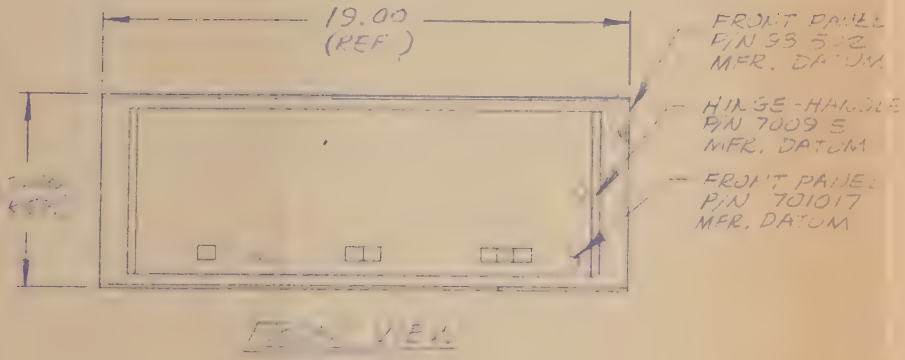
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



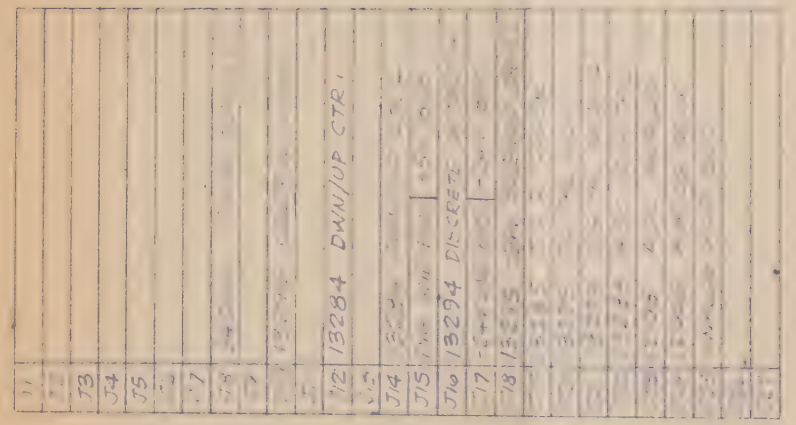
TOP VIEW



REAR VIEW



FRONT VIEW



1. HANDSTAMP AND WIRE PER WIRE LIST NO. 800438
NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE
DATA LOGGER SYSTEM

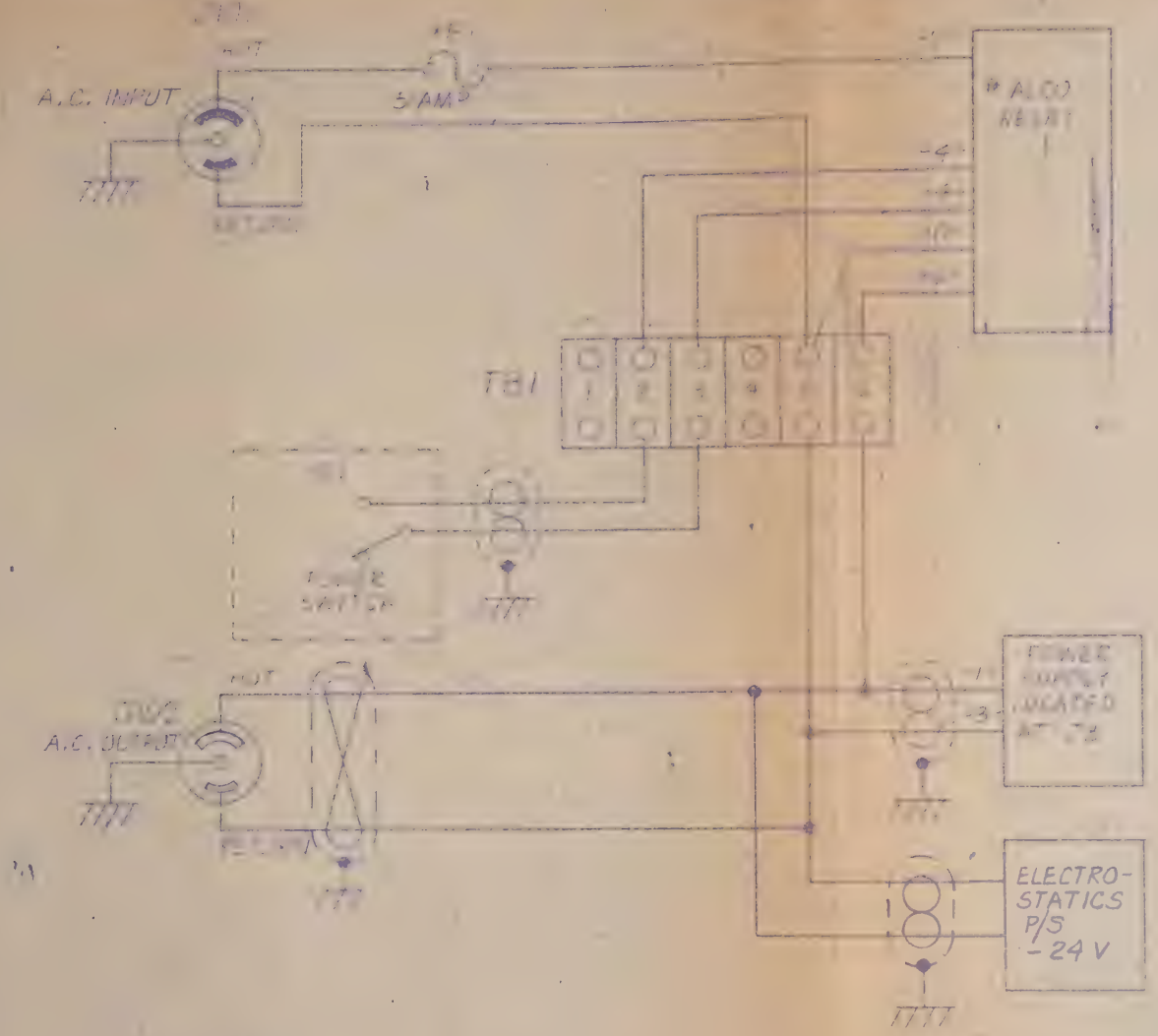
DWN
CHK
SCALE
DES
ENGR
FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE B | 120-131 | REV
SHT 1 OF 2

DIETZGEN 196 MG 10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03 .XXX ± .010 ANGLES ± 1°

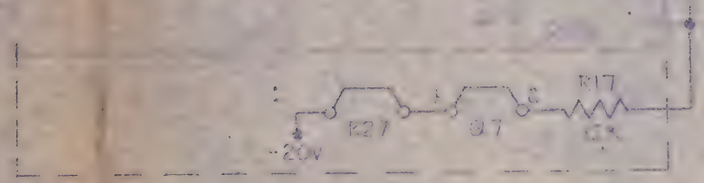
TITLE: ASSY.- DATA LOGGER

datum inc.
178 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	DES
CHK	ENGR
SCALE NONE	ENG 31160

B 120-181

SHT 2 OF 2



NEXT ASSY	DRAFTSMAN	
	CHECKER	
	DESIGNER	
	ENGR	
	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°	

TITLE

8 CHANNEL MULTIPLEXER

SCALE

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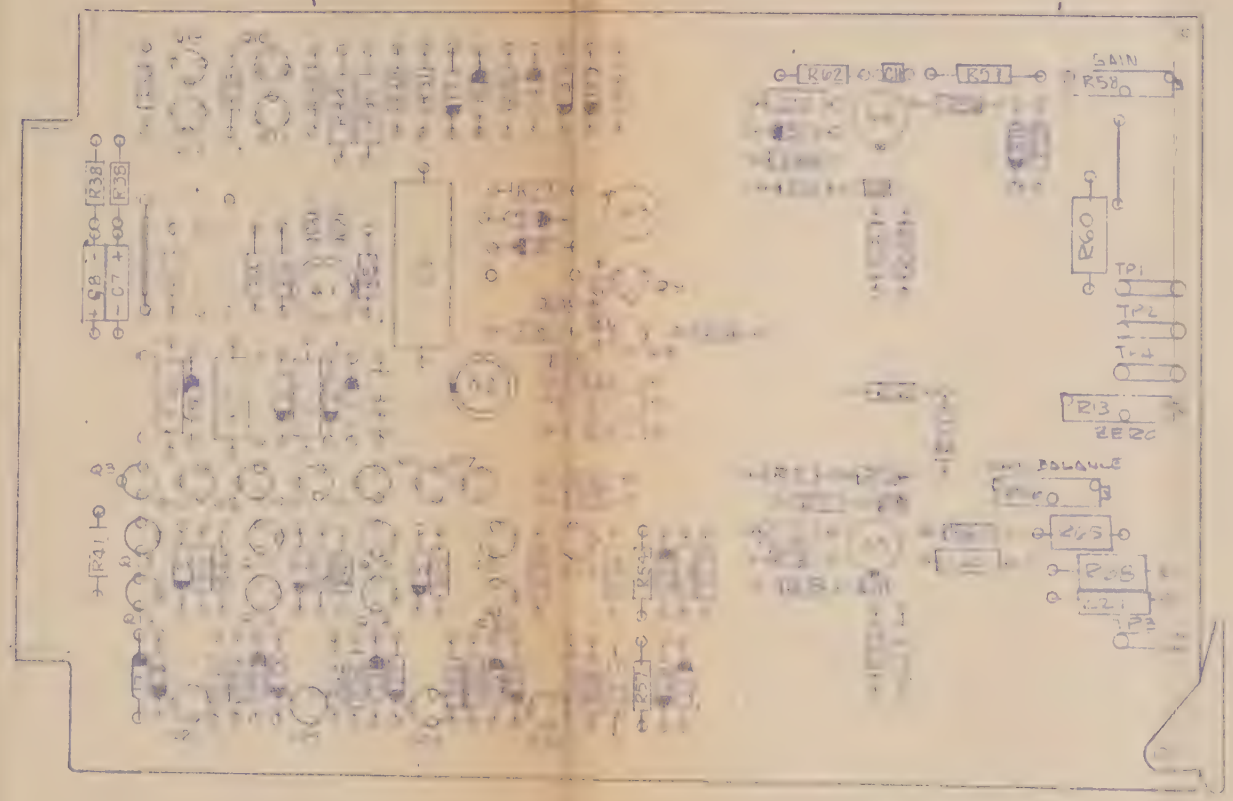
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE | DWG | REF

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ±1/2°

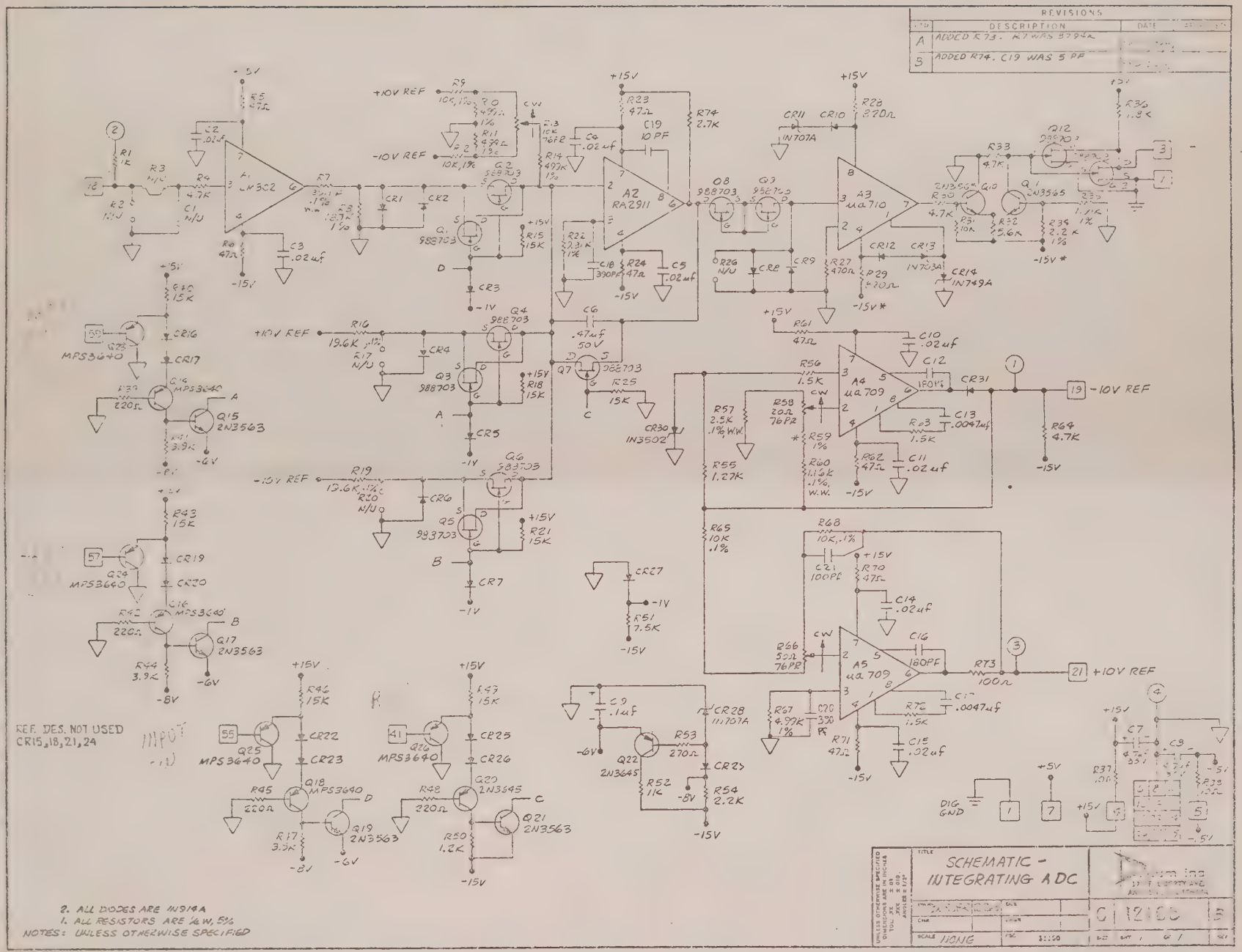
TITLE
1-INTEG
DC

DWN	3-12-70	DES	
CHK		ENGR	
SCALE		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 12108 | C
SIZE | SHT OF | REV

DIETZGEN 196MG-10


REVISIONS
LTR | DESCRIPTION | DATE
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B | ADDED R74. C19 WAS 5 PF
+5V
-5V
+15V
-15V
+10V REF
-10V REF
-15V REF
A1 LM302
A2 RA2911
A3 ua710
A4 ua709
A5 ua709
Q1 2N3563
Q2 2N3563
Q3 2N3563
Q4 2N3563
Q5 2N3563
Q6 2N3563
Q7 2N3563
Q8 2N3563
Q9 2N3563
Q10 2N3563
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Q18 MPS3640
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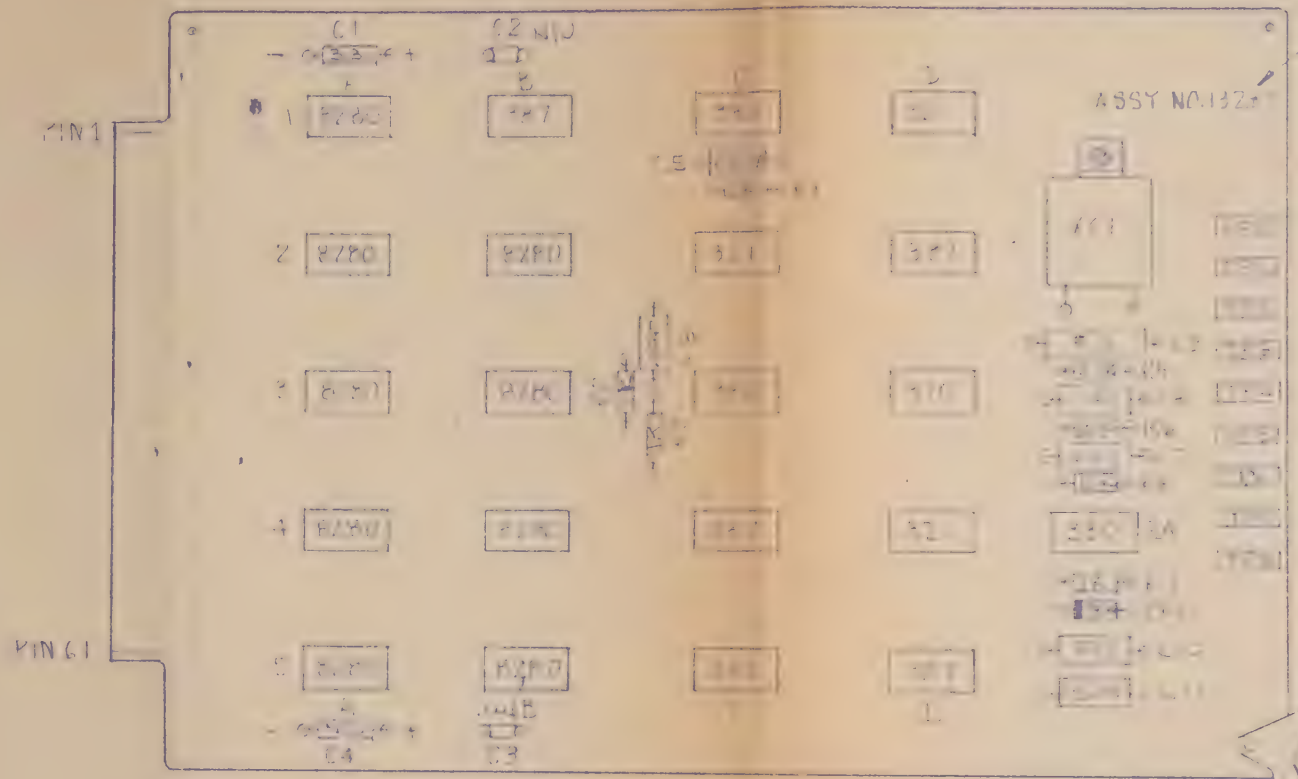
Q20 2N3645
Q21 2N3563
Q22 2N3645
Q23 MPS3640
Q24 MPS3640
Q25 MPS3640
Q26 MPS3640
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR10 IN707A
CR11 IN707A
CR12 IN703A
CR13 IN703A
CR14 IN749A
CR27
CR28 IN707A
CR30 IN3502
R1 1K
R2 N/U
R3 N/U
R4 4.7K
R5 47Ω
R6 47Ω
R7 8.79K 1%
R8 8.87K 1%
R9 10K 1%
R10 47Ω 1%
R11 499Ω 1%
R12 10K 1%
R13 10K 76PR
R14 499K 1%
R15 15K
R16 19.6K 1%
R17 N/U
R18 15K
R19 19.6K 1%
R20 N/U
R21 15K
R22 2.21K 1%
R23 47Ω
R24 47Ω
R25 15K
R26 N/U
R27 470Ω
R28 270Ω
R29 470Ω
R30 4.7K
R31 10K
R32 5.6K
R33 47K
R34 1.8K
R35 2.2K 1%
R36 1.21K 1%
R37 10K
R38 15K
R39 220Ω
R40 15K
R41 3.9K
R42 220Ω
R43 15K
R44 3.9K
R45 220Ω
R46 15K
R47 220Ω
R48 220Ω
R49 15K
R50 1.2K
R51 7.5K
R52 1K
R53 270Ω
R54 2.2K
R55 1.27K
R56 1.5K
R57 2.5K .1% W.W.
R58 20Ω 76PR
R59 1%
R60 1.16K .1% W.W.
R61 47Ω
R62 47Ω
R63 1.5K
R64 4.7K
R65 10K .1%
R66 50Ω 76PR
R67 4.99K 1%
R68 10K .1%
R70 47Ω
R71 47Ω
R72 1.5K
R73 100Ω
C1 N/U
C2 .02uf
C3 .02uf
C4 .02uf
C5 .02uf
C6 .47uf 50V
C7 4.7uf 35V
C8 .1uf
C9 .1uf
C10 .02uf
C11 .02uf
C12 150PF
C13 .0047uf
C14 .02uf
C15 .02uf
C16 180PF
C17 .0047uf
C18 390PF
C19 10 PF
C20 330 PF
C21 100PF
R39 N/U
R30 N/U
R37 10Ω
R38 10Ω
R39 10Ω
A
B
C
D
1
2
3
4
5
7
19 -10V REF
21 +10V REF
55
57
59
41
DIG GND
REF. DES. NOT USED
CR15, 18, 21, 24
2. ALL DIODES ARE IN916A
1. ALL RESISTORS ARE ¼W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED
TITLE
SCHEMATIC - INTEGRATING ADC
SCALE NONE
SIZE C
DWG NO 12108
REV B
SHT 1 OF 1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE ASSY— INTEGRATING ADC LOGIC

DWN [illegible] DES [illegible]

CHK ENGR

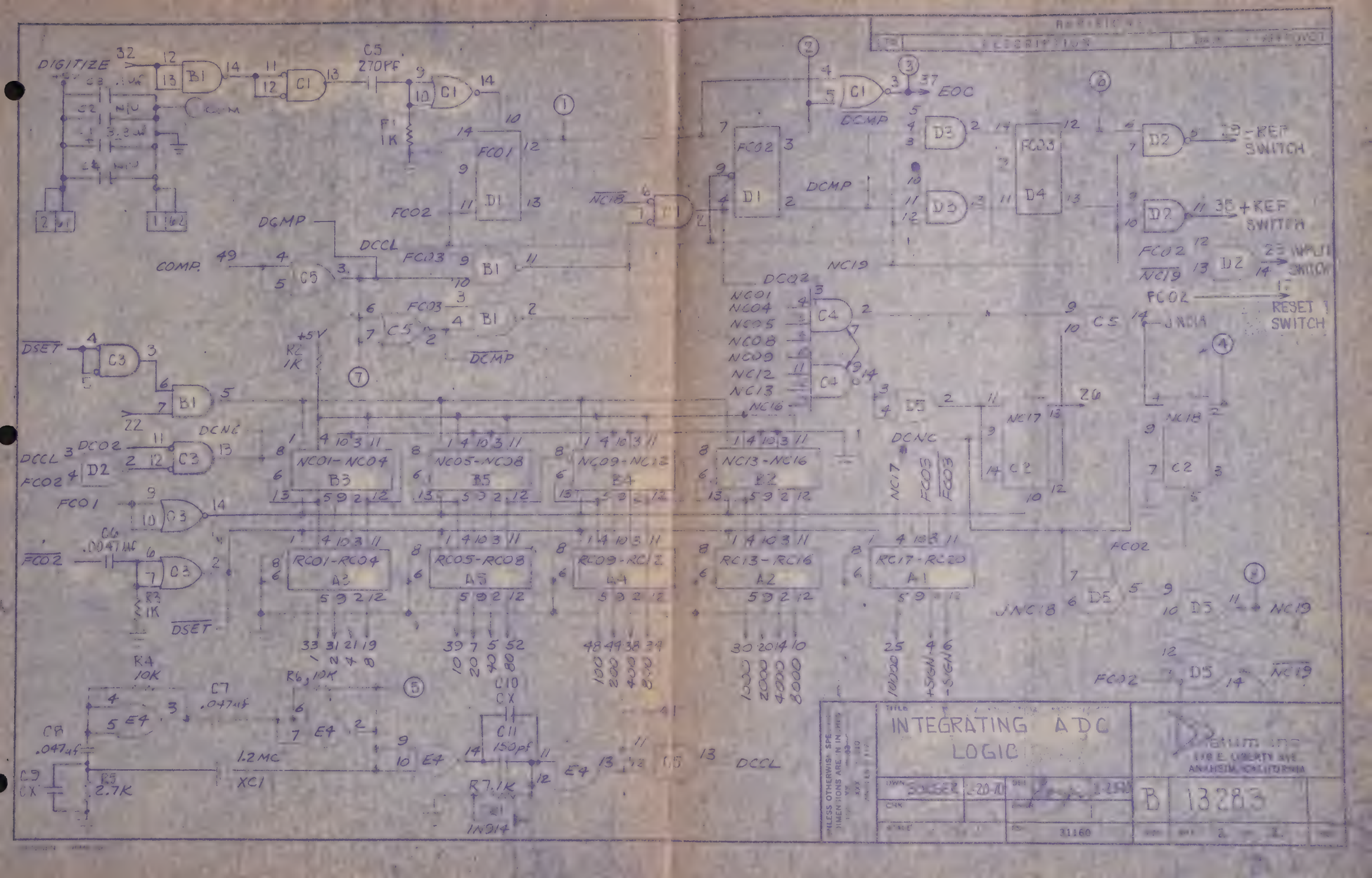
SCALE [illegible] FSC 31160

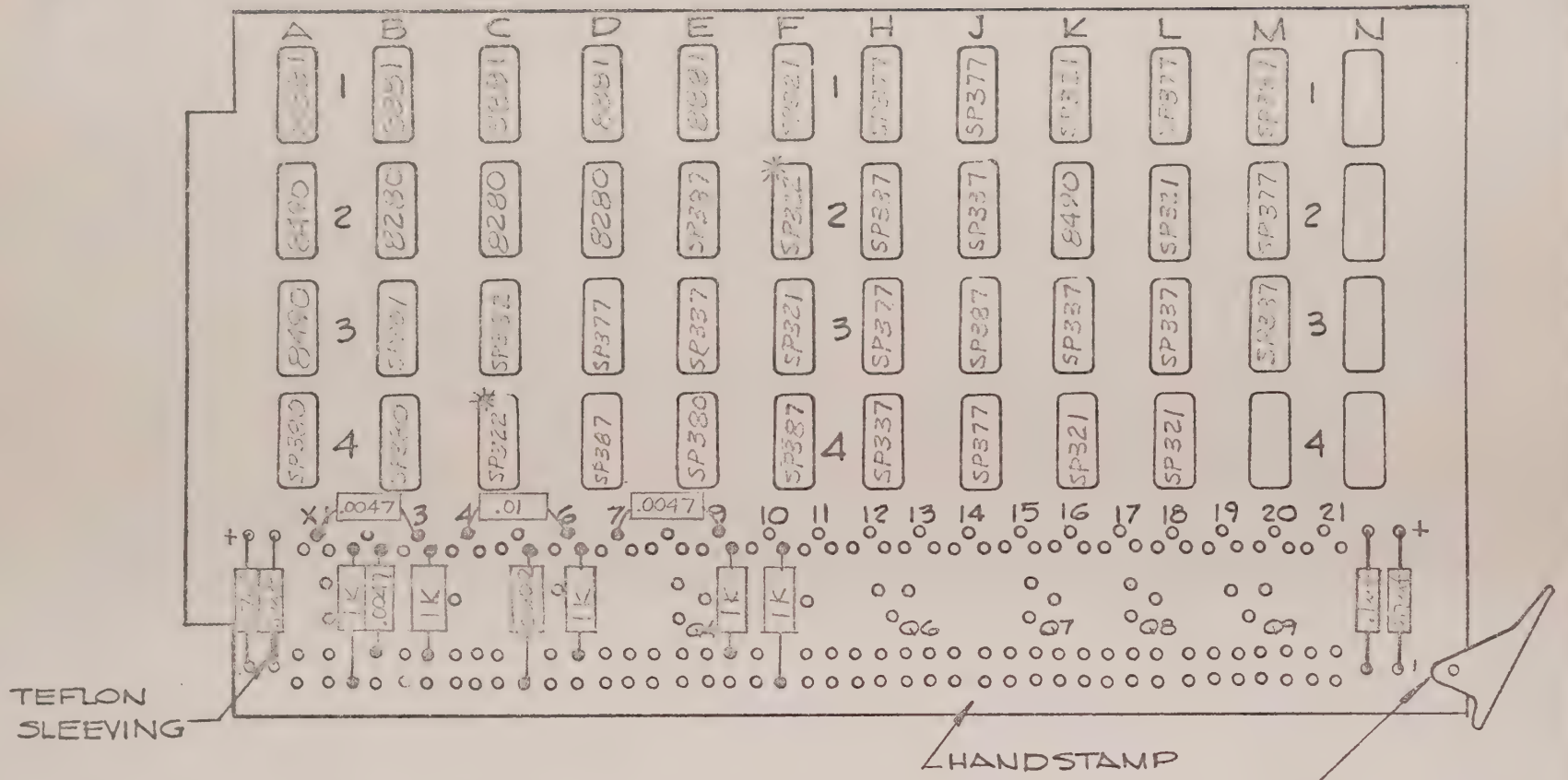
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B 15283

SIZE SHT 1 OF 2 REV

DIETZGEN 196 MG-10-


DIGITIZE
32
B1
C1
C5
270PF
R1
1K
FCO1
FCO2
FCO3
DCMP
DCCL
COMP.
49
C5
NC18
DSET
C3
+5V
R2
1K
22
DCO2
DCNC
D2
NC01-NC04
B3
NC05-NC08
B5
NC09-NC12
B4
NC13-NC16
B2
C6
.0047MF
R3
1K
RC01-RC04
A3
RC05-RC08
A5
RC09-RC12
A4
RC13-RC16
A2
RC17-RC20
A1
R4
10K
R6, 10K
C7
.047uf
C8
.047uf
C9
CX
R5
2.7K
1.2MC
XC1
C10
CX
C11
150pf
R7 1K
IN914
33 31 21 19
1 2 4 8
39 7 5 52
10 20 40 80
48 49 38 34
100 200 400 800
30 20 14 10
1600 2000 4000 8000
25
100000
+SIGN
-SIGN
6
EOC
37
D3
D4
D5
FCO3
+REF SWITCH
35
-REF SWITCH
23
INPUT SWITCH
RESET SWITCH
JNC18
NC19
NC17
NC16
NC13
NC12
NC09
NC08
NC05
NC04
NC01
Z6
C4
C2
E4
INTEGRATING ADC LOGIC
B
13283
31160



2. * DENOTES 16 PIN IC SOCKET.
1. TOP SOLDER CAPACITORS C1, C2, C4

NOTES:
UNLESS OTHERWISE SPECIFIED

NEXT ASSY

DRAFTSMAN CMS	1-15-70	
CHECKER		
DESIGNER		
ENGR		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE

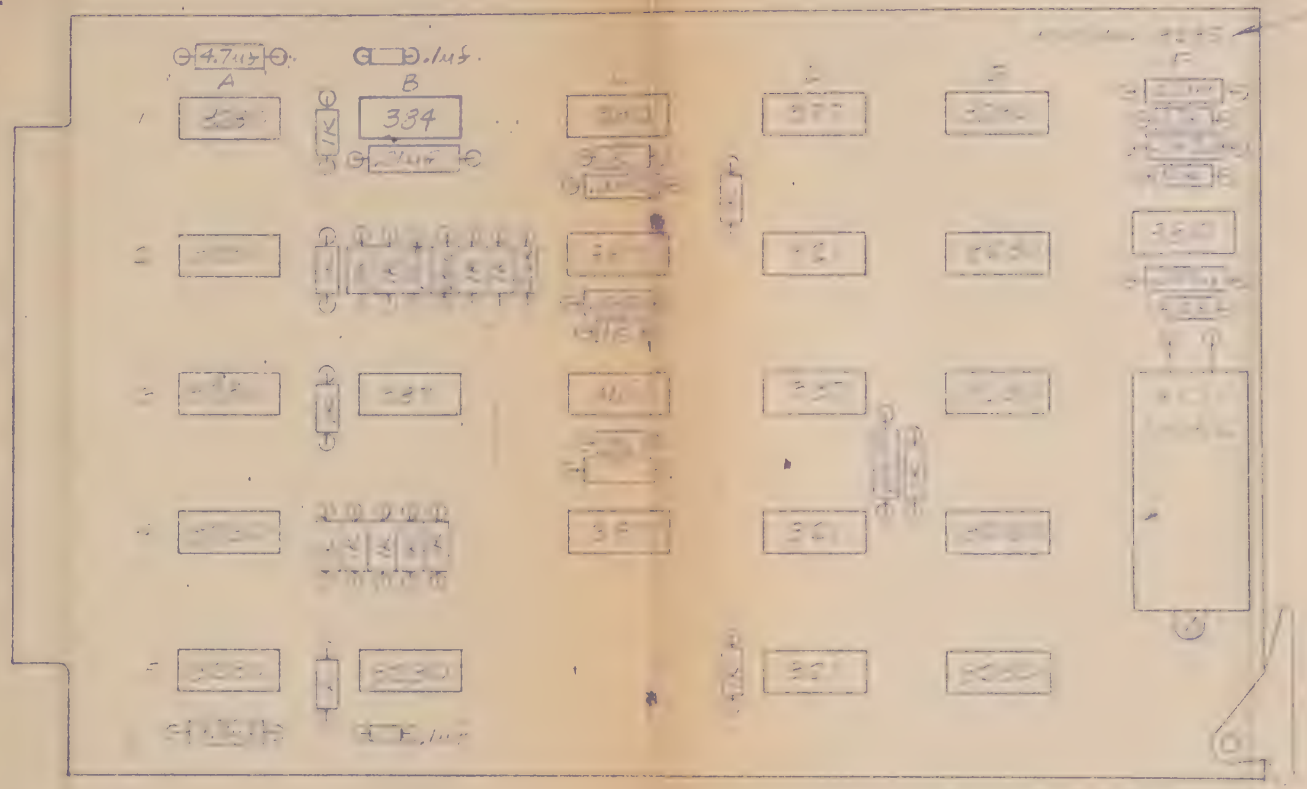
DOWN/UP COUNTER

SCALE NONE

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

A	13284	
SIZE	SHT 1 OF 1	REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



1. ALL RESISTORS ARE 1/4W, 5%

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .03
XXX ± .010
ANGLES ± 1/2°

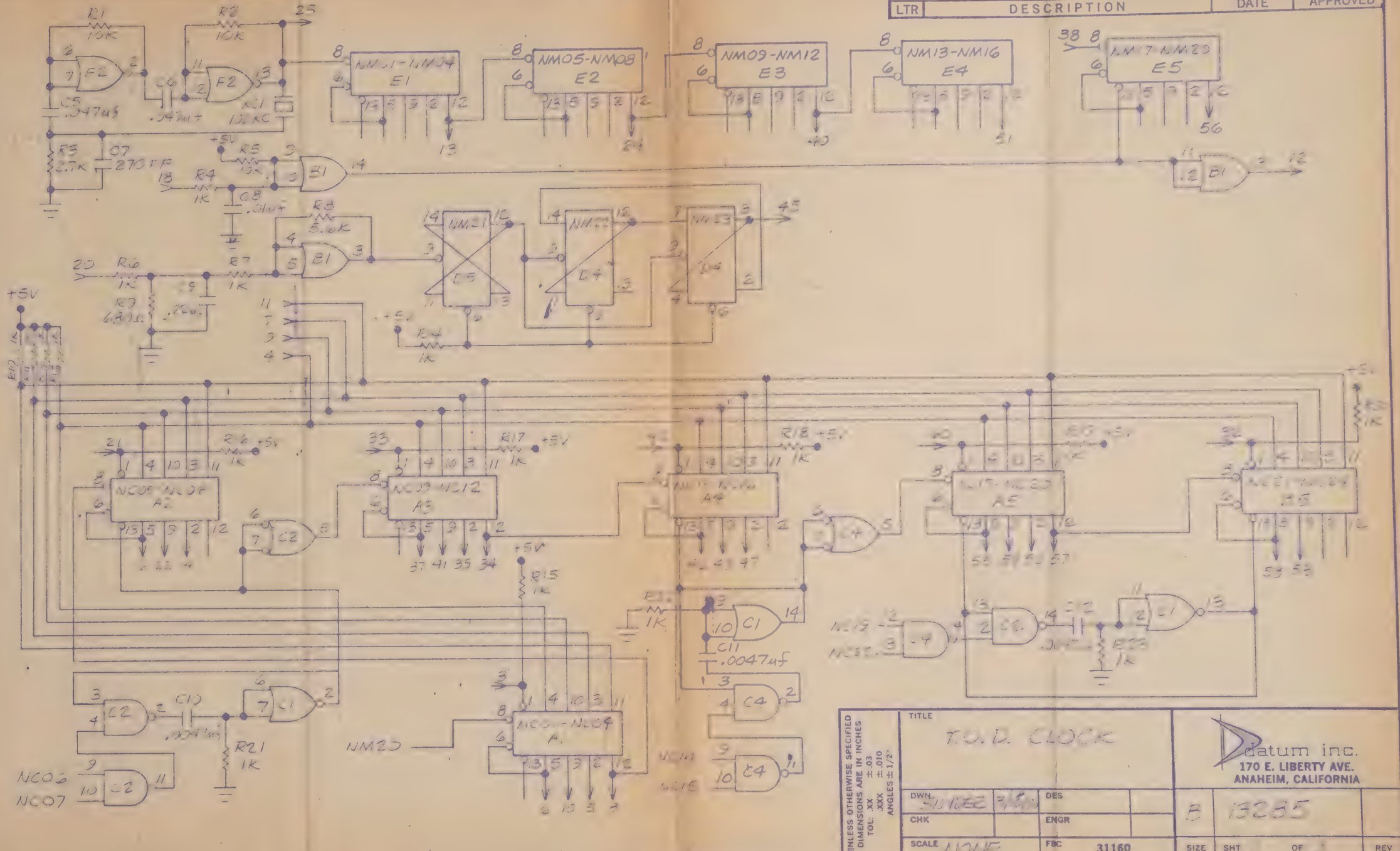
TITLE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	DES		
CHK	ENGR		
SCALE	FSC 31160	SIZE	SHT 1 OF 1

DIETZGEN 196MG 10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ±.03 XXX ±.010 ANGLES ±1/2°

TITLE: T.O.D. CLOCK

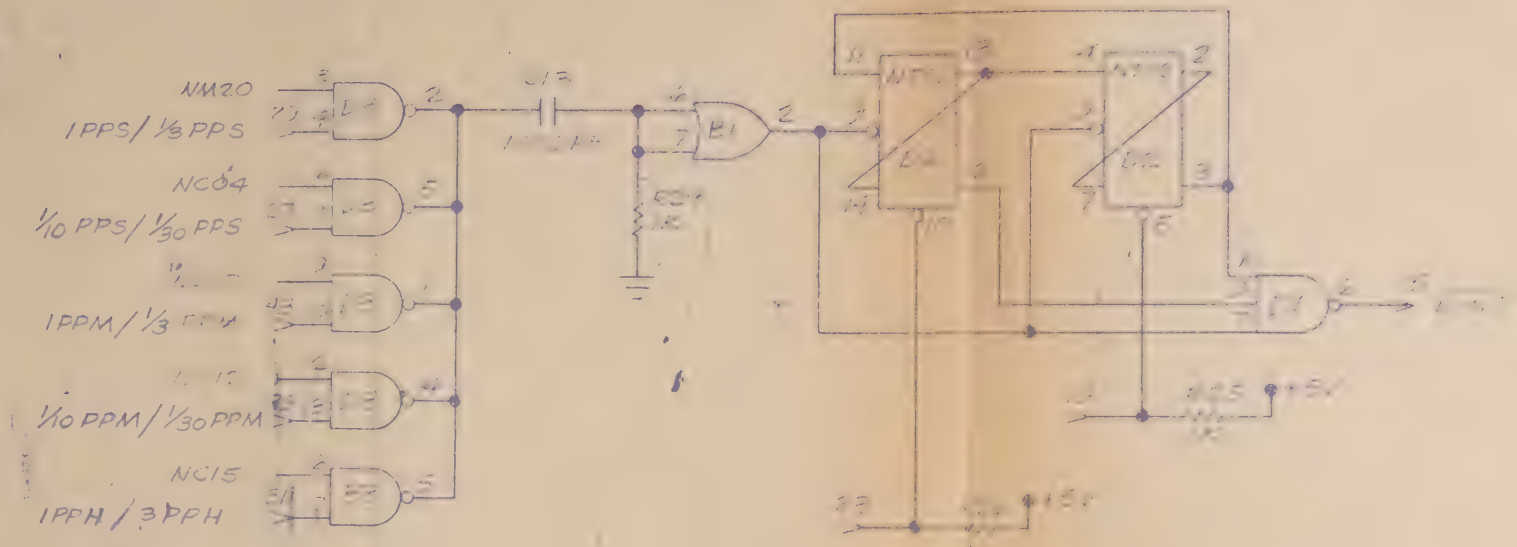
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

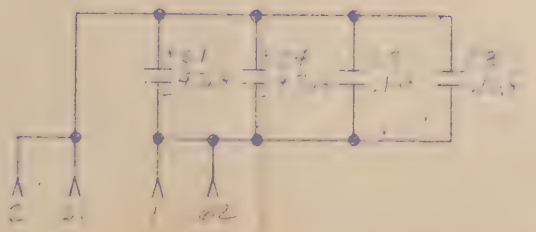
DWN.	DES
CHK	ENGR
SCALE NONE	FSC 31160

SIZE	SHT	OF	REV
B	13285		

DIETZGEN 196MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE 7.0 CLOCK

DWN [illegible] DES

CHK ENGR

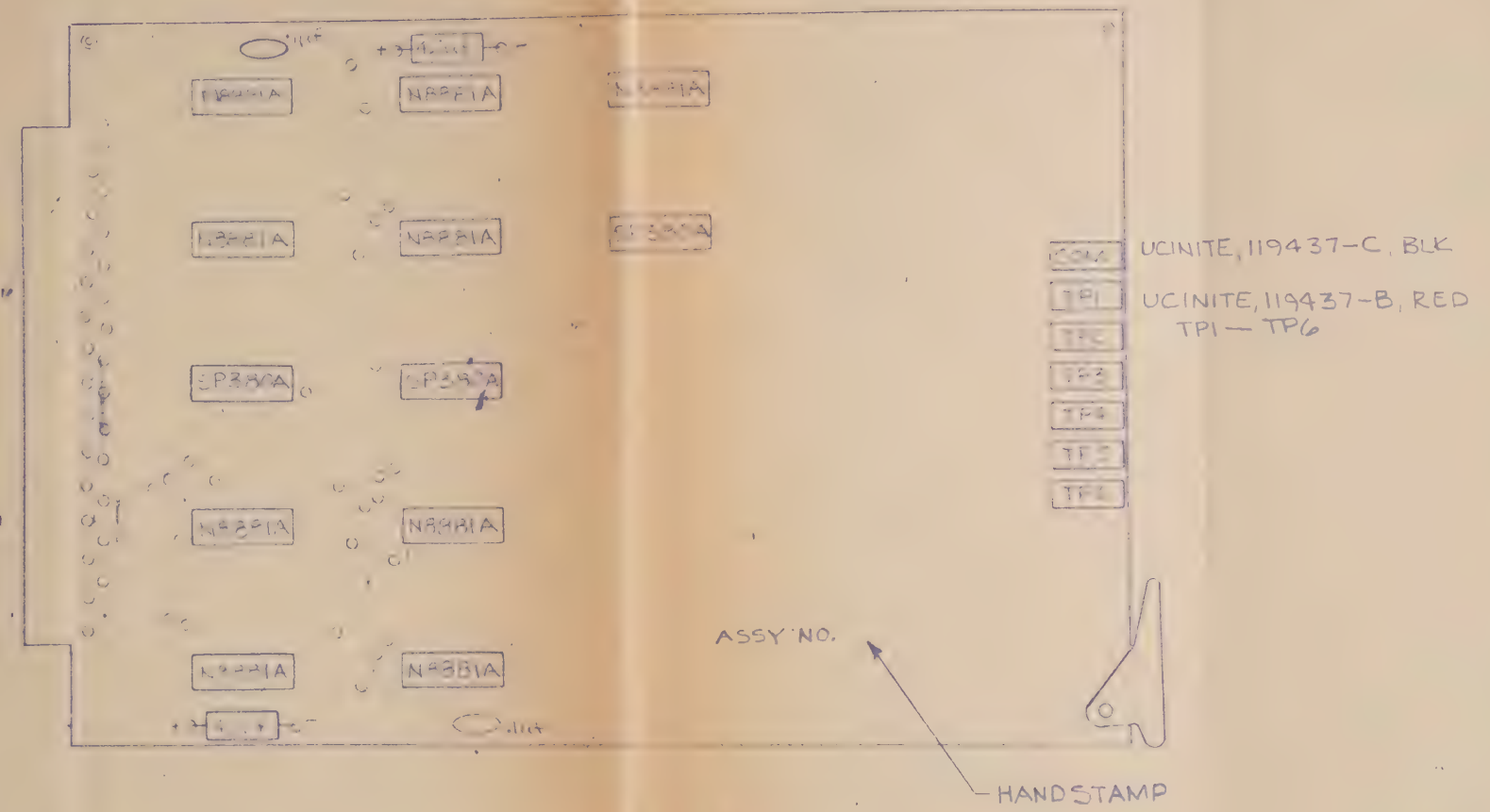
SCALE 1.5/1 FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B 13095

SIZE SHT 3 OF 3 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ±1/2°

TITLE: DIGITAL MUX ASSY.

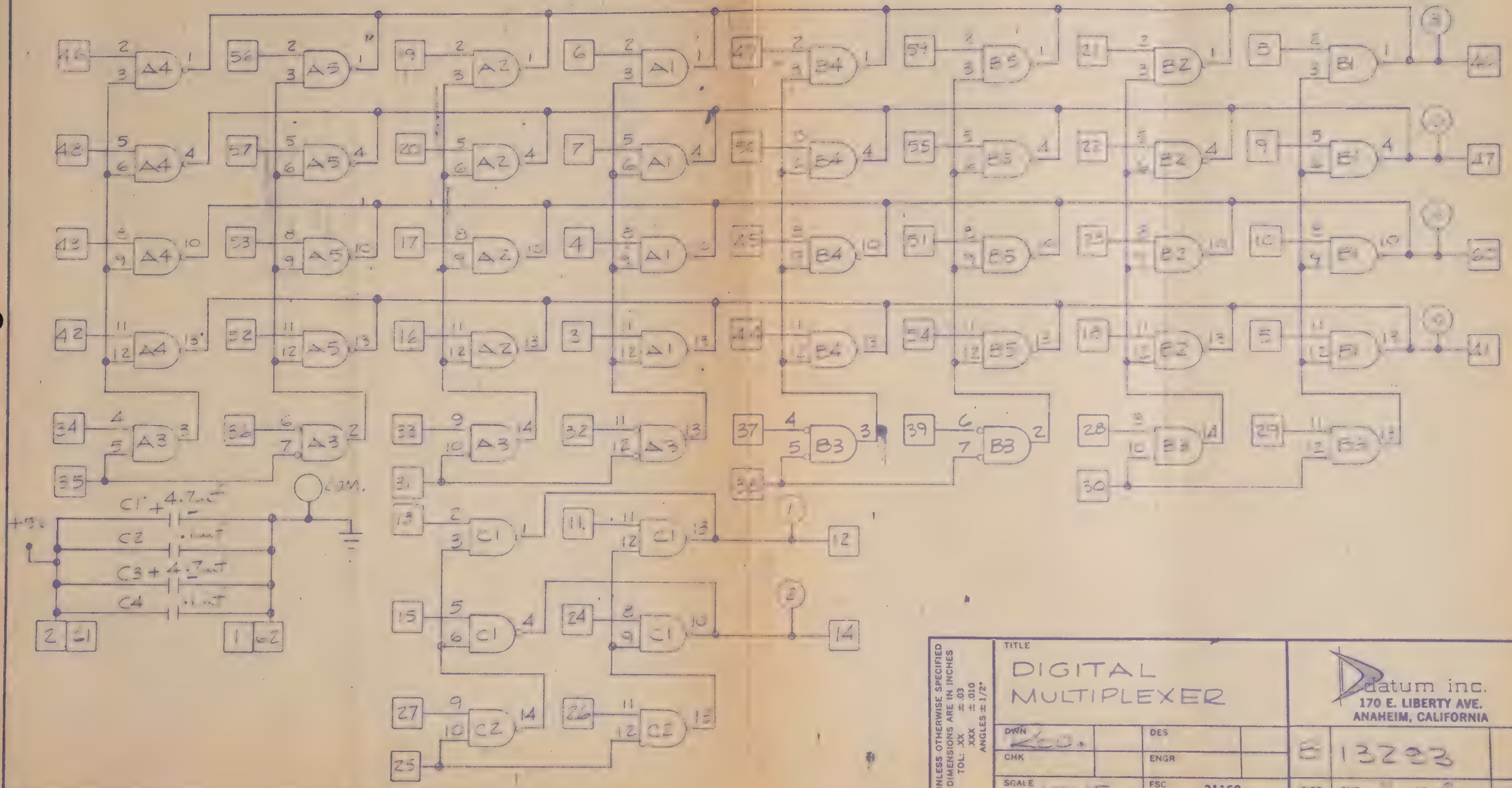
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	CHK	DES	ENGR	SCALE	FSC	SIZE	SHT	REV
MARTINEZ 2/13/71				F1 —	31160	B	1 OF 2	

13293

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



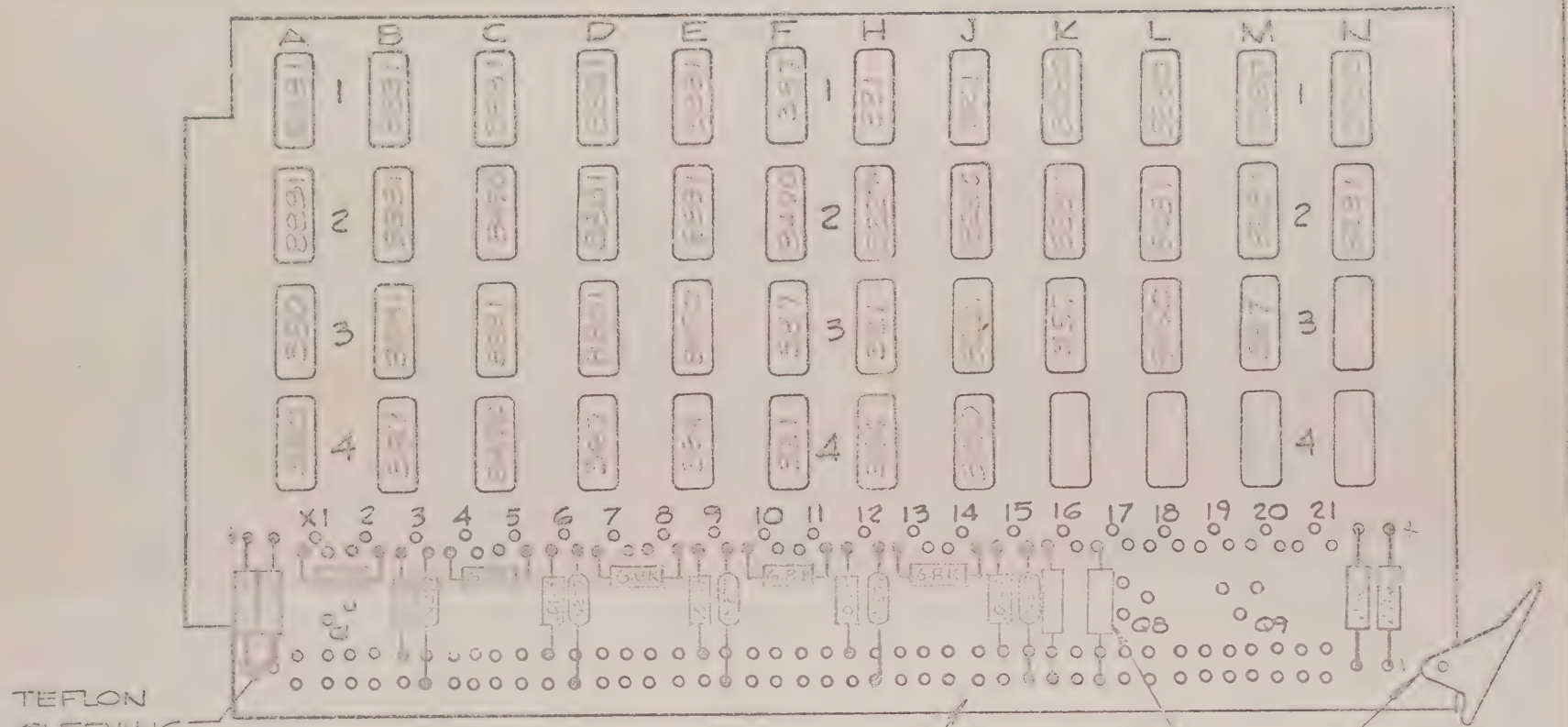
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03 .XXX ±.010 ANGLES ± 1/2°

TITLE
DIGITAL MULTIPLEXER

DWN		DES	
CHK		ENGR	
SCALE NONE		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE	SHT	OF	REV
B	13293		


A B C D E F H J K L M N
1 2 3 4
X1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
C8
C9
TEFLON SLEEVING
HANDSTAMP
FACTORY SELECT
STANFORD APPLIED ENGINEERING P-6100

2. * DENOTES 16 I.C. SOCKET

1. TOP SOLDER CAPACITORS C1, C2, C4

NOTES:
UNLESS OTHERWISE SPECIFIED

DRAFTSMAN		1-27-70
CHECKER		
DESIGNER		
ENGR		

NEXT ASSY

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

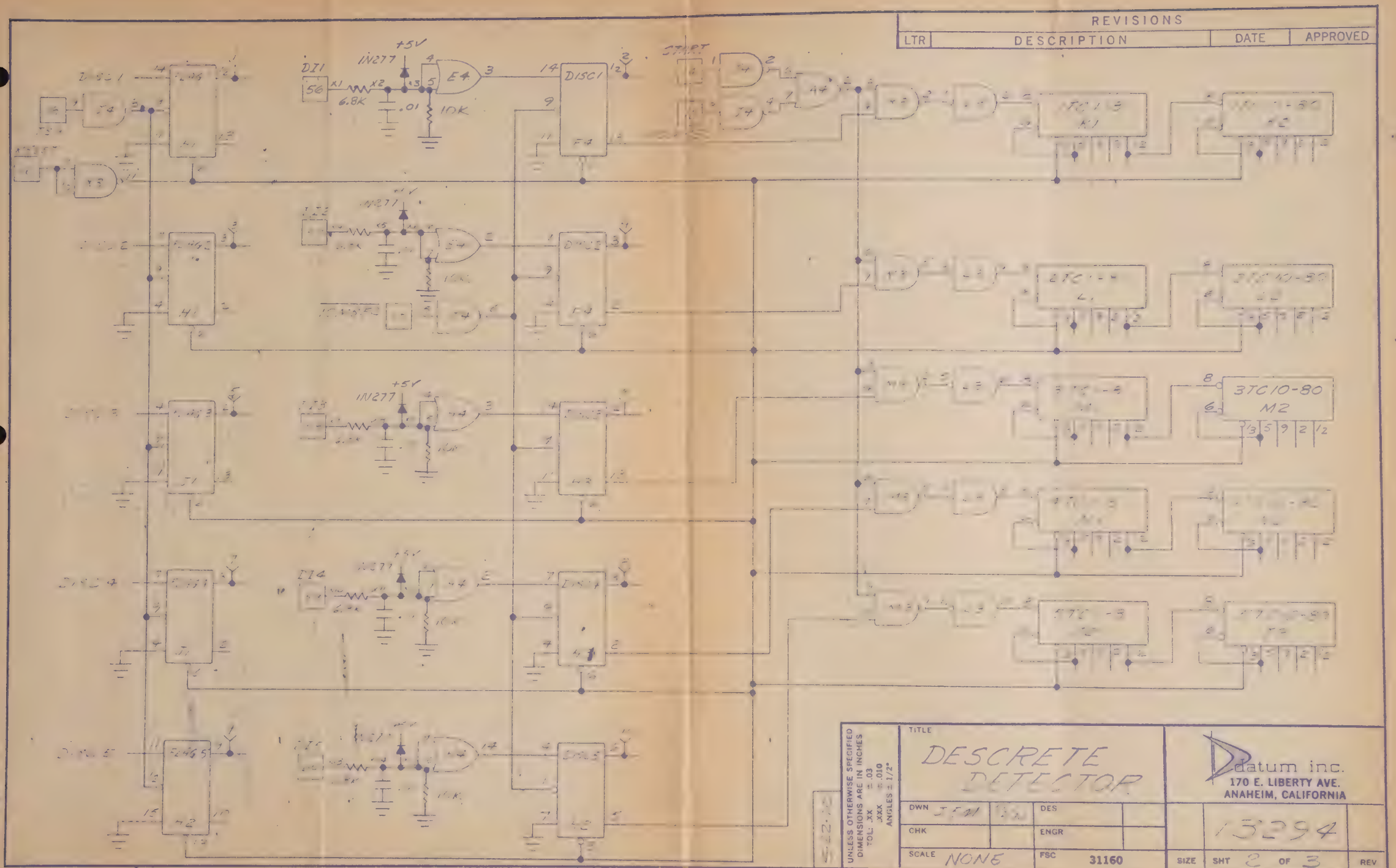
TITLE
DISCRETE DETECTOR

SCALE NONE

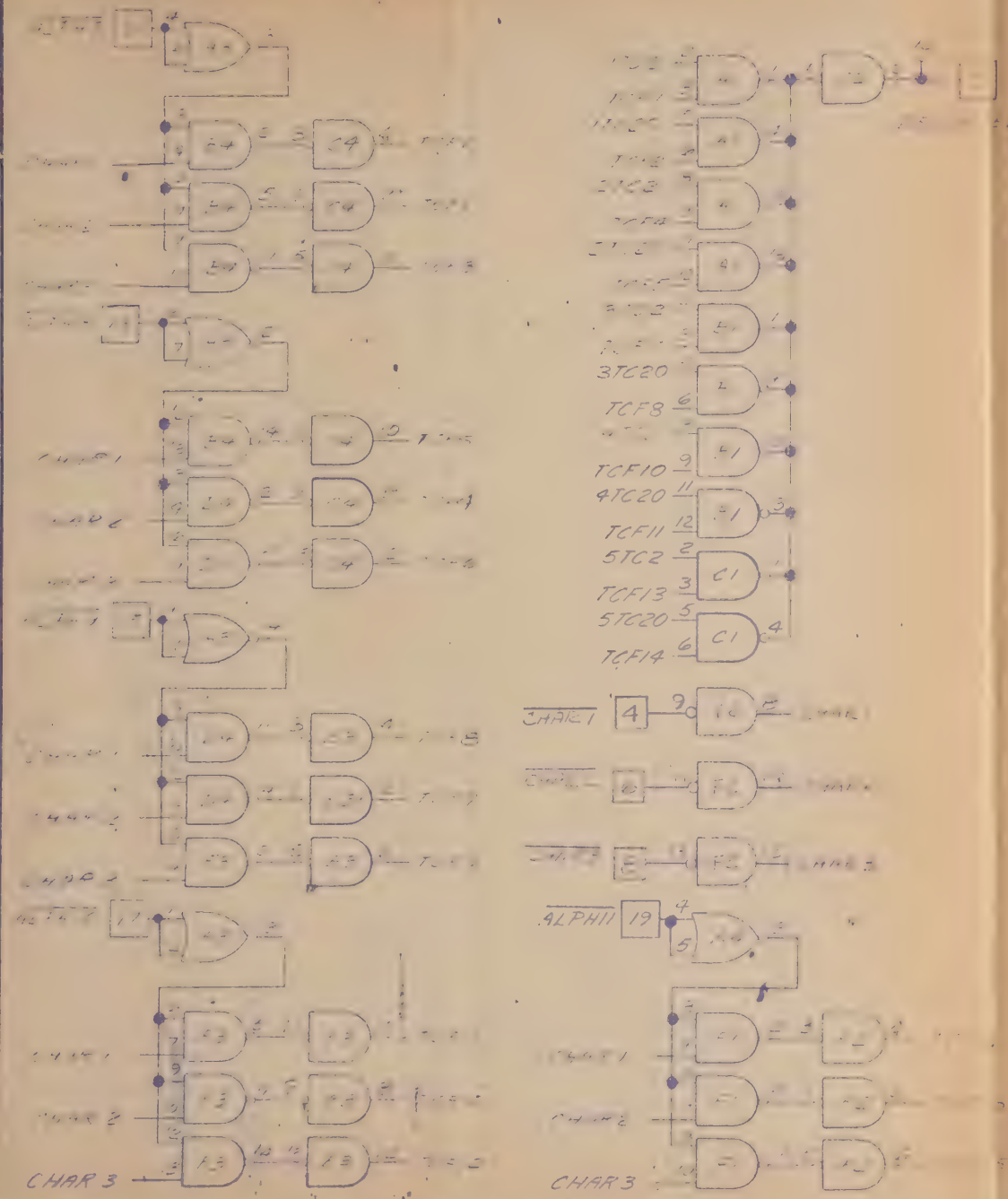
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

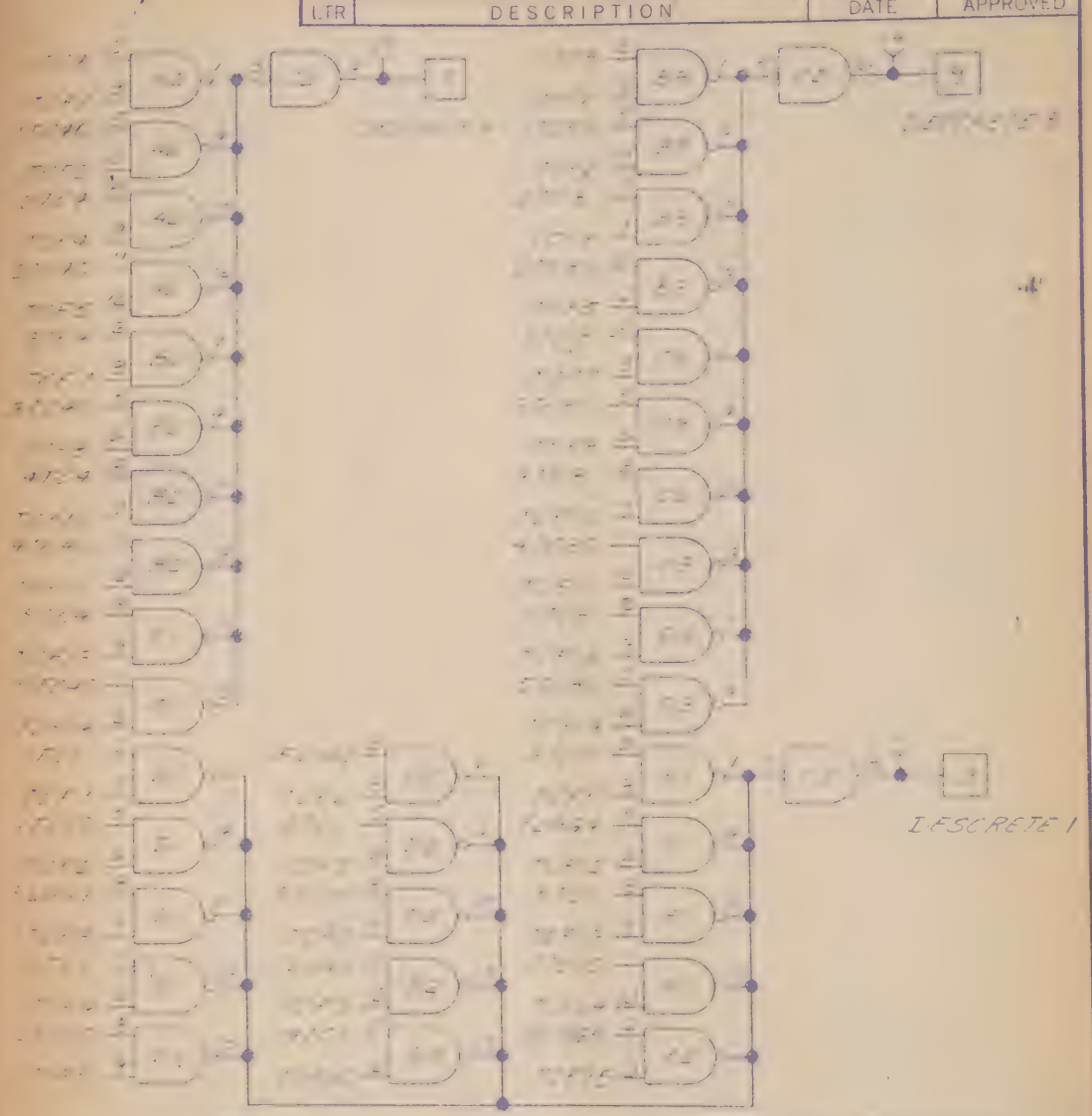
A 13294

SIZE | SHT 1 OF 1 | REV



DIETZGEN 196 MG 10





REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ± 1/2°

TITLE

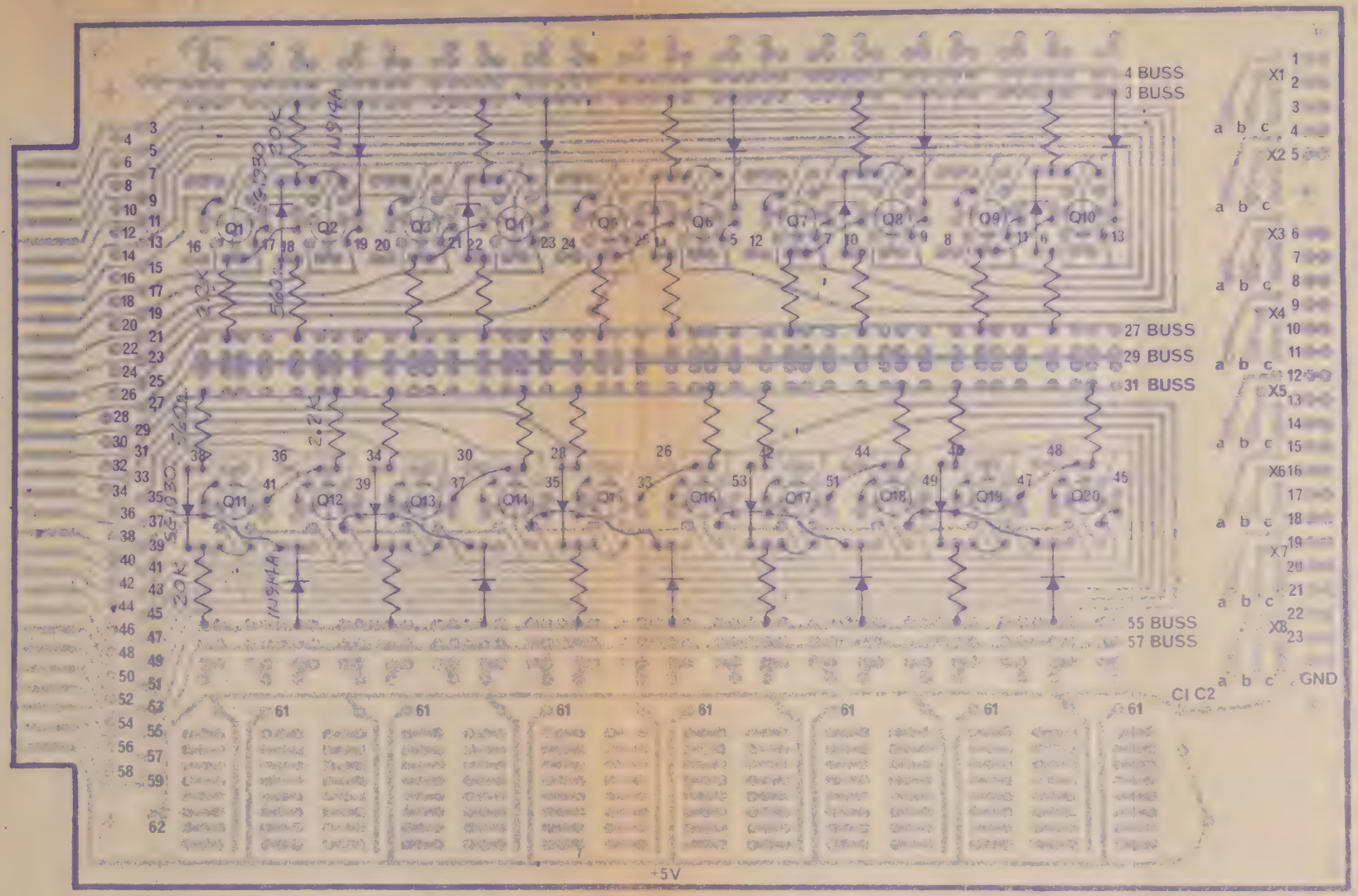
DESCRETE DETECTOR

DWN	J.E.M.	5/2/70	DES	
CHK			ENGR	
SCALE	NONE		FSC	31160

SIZE | SHT | OF | REV

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DIETZGEN 196 MG-10



2. ALL TRANSISTORS ARE 2N2905A
1. ALL RESISTORS ARE ¼W, 5%
NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .03
XXX ± .010
ANGLES ± 1/2°

TITLE
ALT -
-24 V SOLENOID DRIVERS

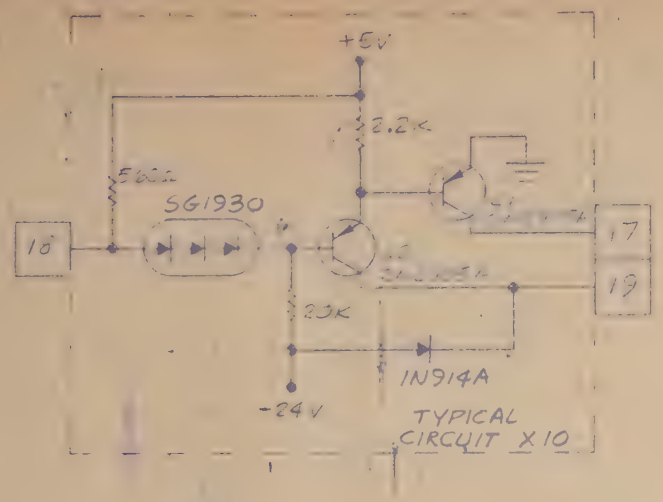
DES
ENGR
DR
3186

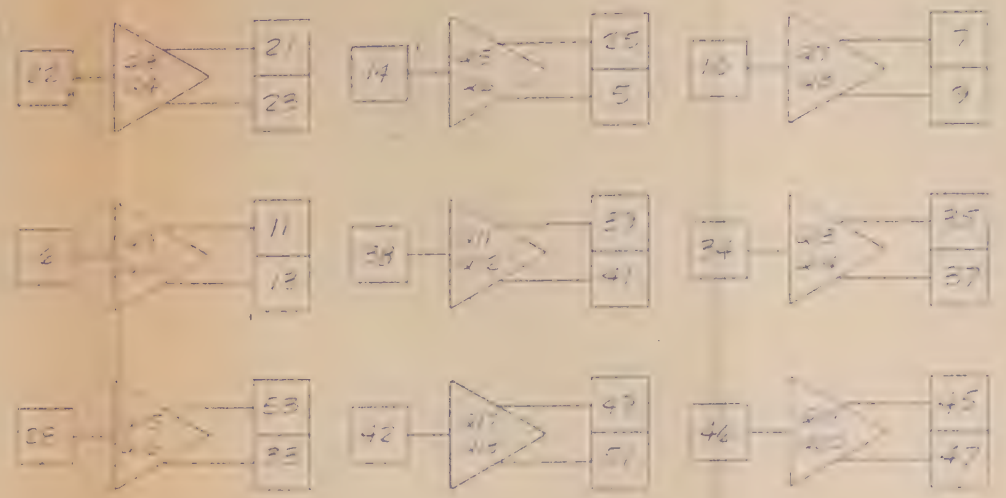
datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

2 3345

SHT 1 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



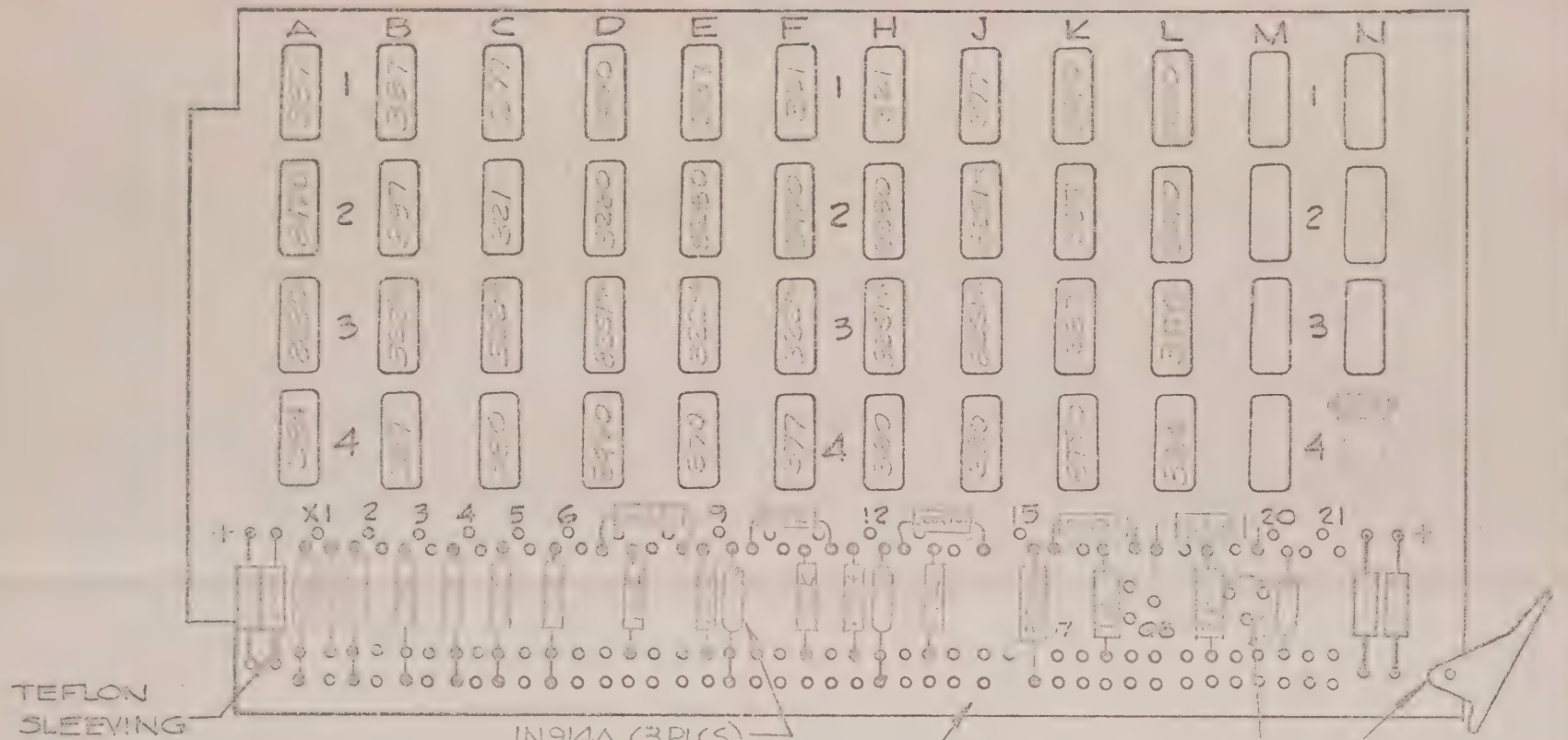


UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ±1/2°

TITLE
SCHEMATIC -
-24 V SOLENOID DRIVERS

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN		DES			
CHK		ENGR		B	13015
SCALE NONE		FSC 31160		SIZE	SHT 1 OF 1 REV



3,4 DENOTES 14 PIN IC SOCKET

1. TOP SOLDER CAPACITORS C1, C2, C4

NOTES:
UNLESS OTHERWISE SPECIFIED

NEXT ASSY

DRAWN		
CHECKER		
DESIGNER		
ENGR		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

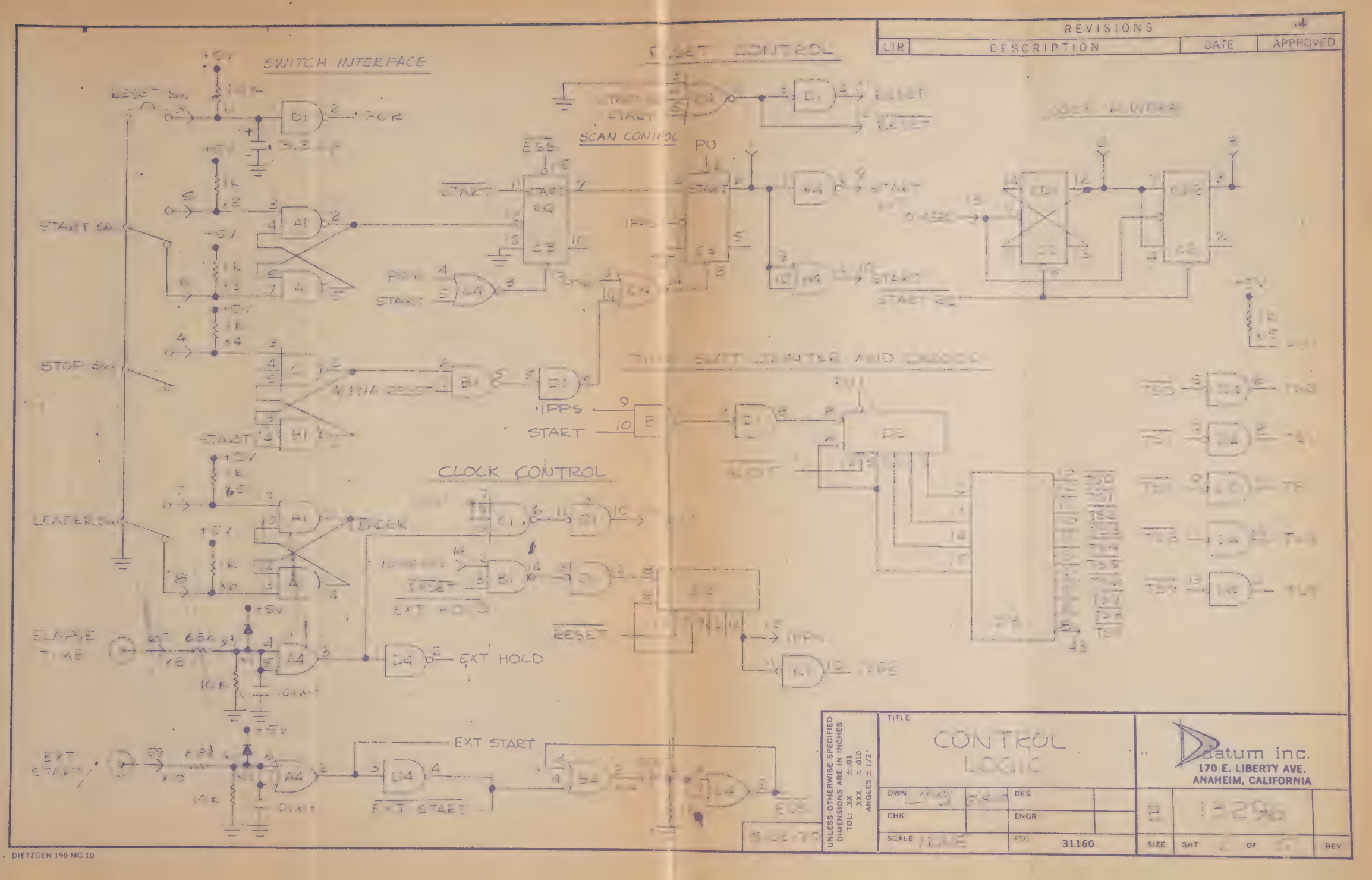
TITLE

CONTROL LOGIC

SCALE NONE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE	DWG	SHT 1 OF	REV
A	13296		



REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

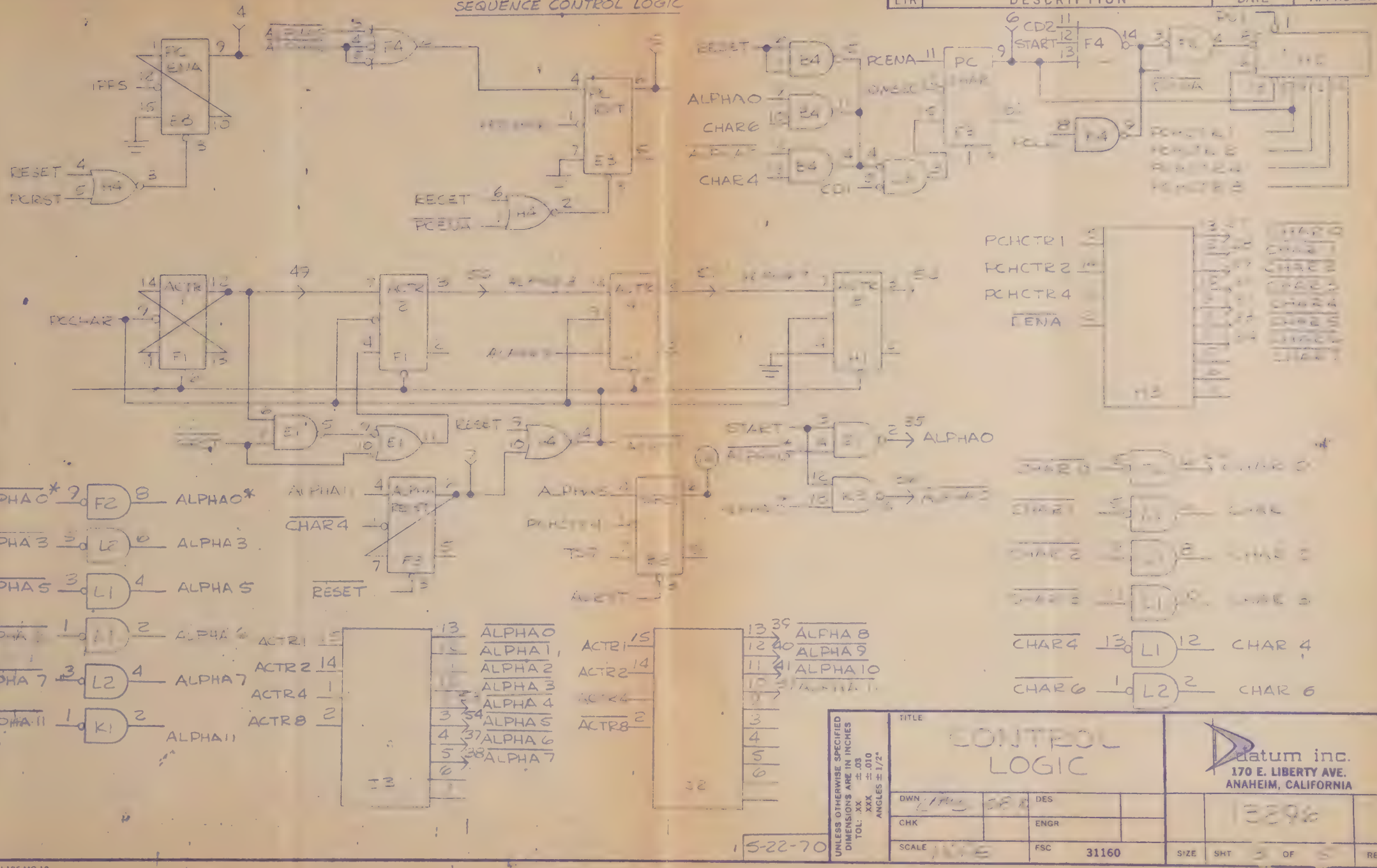
DWN		DES	
CHK		ENGR	
SCALE		FSC 31160	

SIZE | SHT | OF | REV

DIETZGEN 196 MG 10

SEQUENCE CONTROL LOGIC

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE	CONTROL LOGIC		
DWN		DES	
CHK		ENGR	
SCALE		FSC 31160	
SIZE	SHT OF	REV	

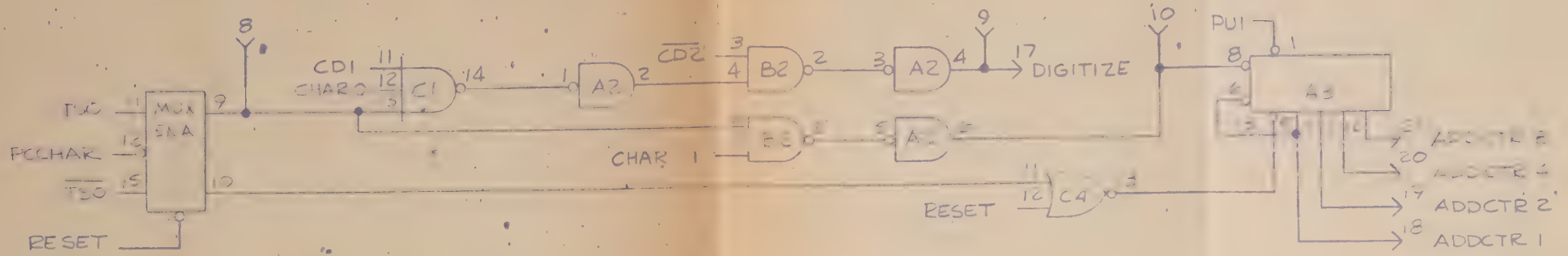
5-22-70

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

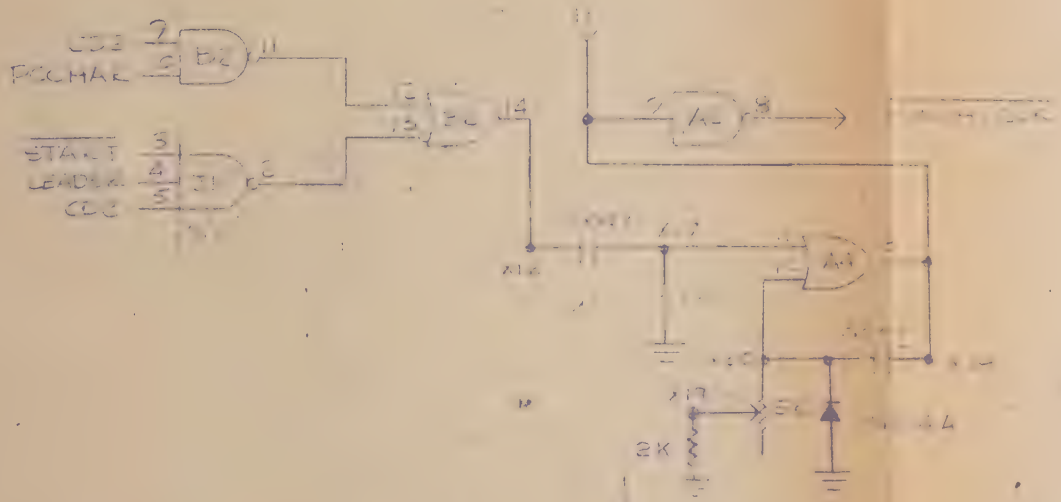
DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

MULTIPLEXER CONTROL



PUNCH CLOCK CONTROL



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: CONTROL LOGIC

DWN LAWS	5-7-80	DES	
CHK		ENGR	
SCALE NONE		FSC 31160	

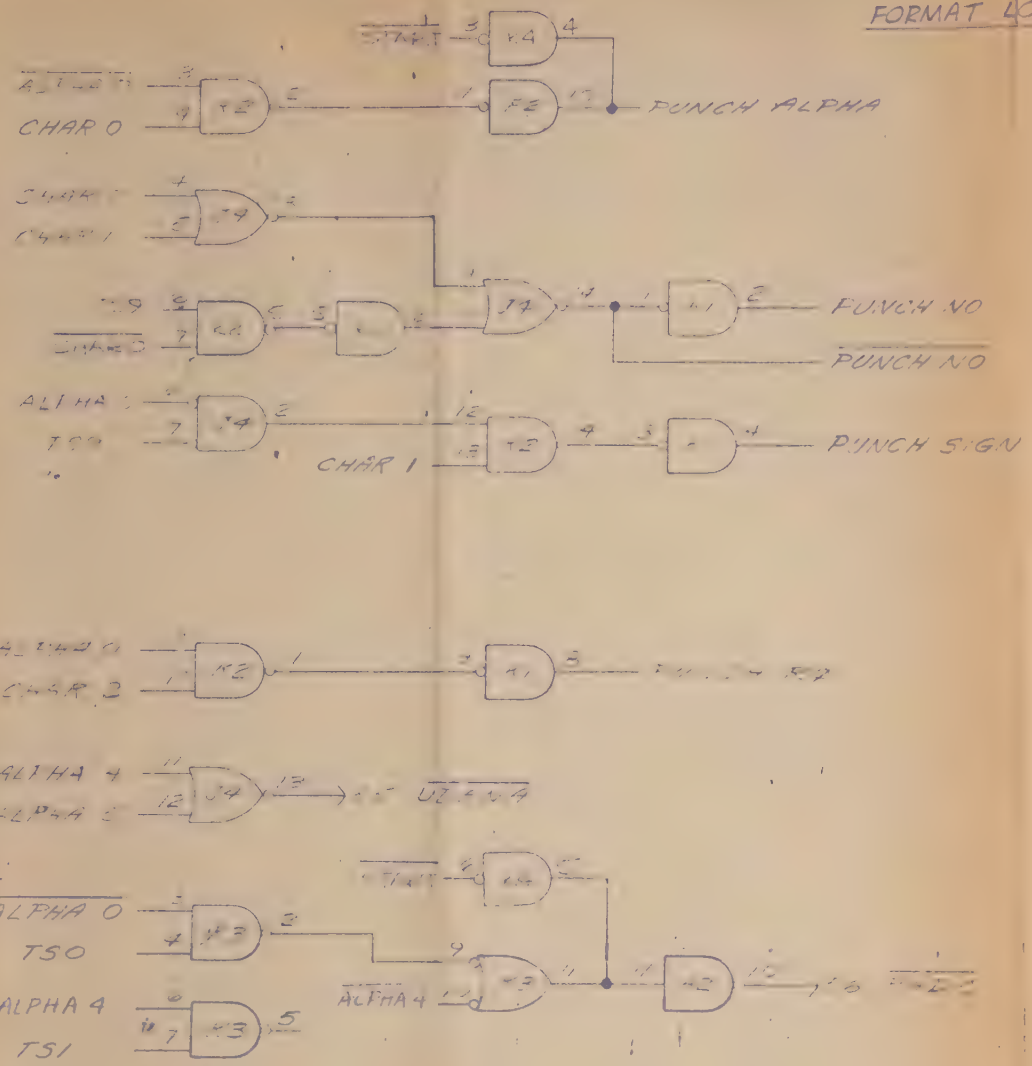
Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

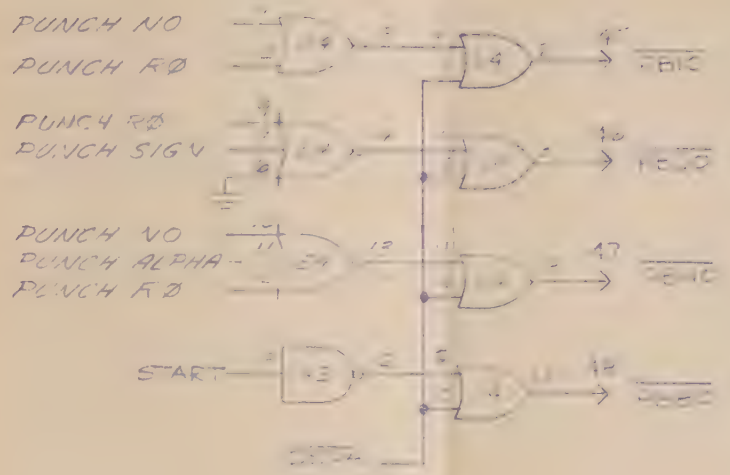
13896

SIZE | SHT 4 OF 5 | REV

DIETZGEN 196 MG 10

FORMAT LOGIC





REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .03
XXX ± .010
ANGLES ± 1/2°

TITLE: CONTROL LOGIC

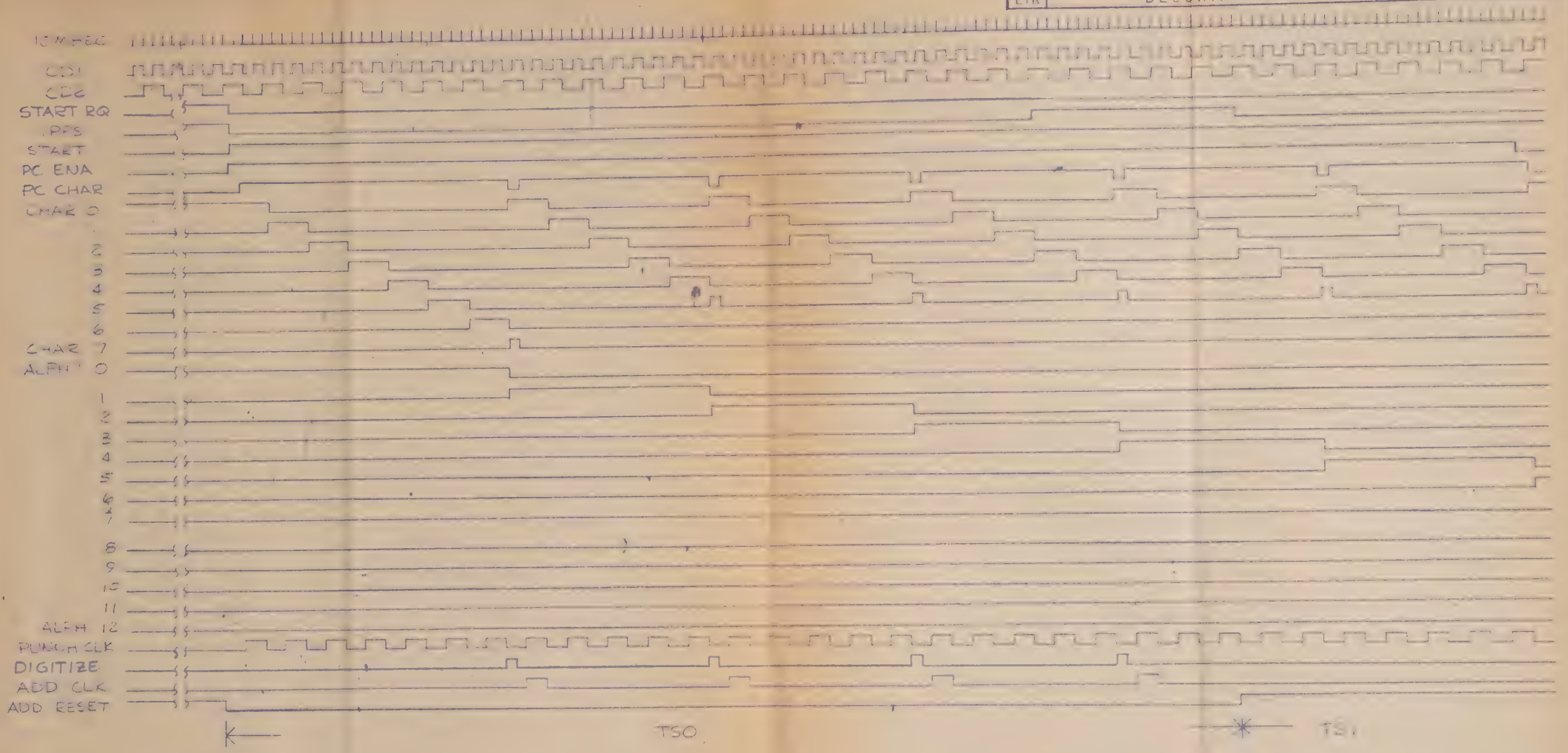
DWN J.E.M. 5/4/70	DES		
CHK	ENGR		
SCALE NONE	FSC 31160	SIZE B	13296

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SHT OF REV

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ± 1/2°

TITLE: TIMING DIAGRAM

DWN		DES	
CHK		ENGR	
SCALE		FSC 31160	

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B	800442	
SIZE	SHT 1 OF 4	REV

DIETZGEN 196 MG-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TIMING DIAGRAM

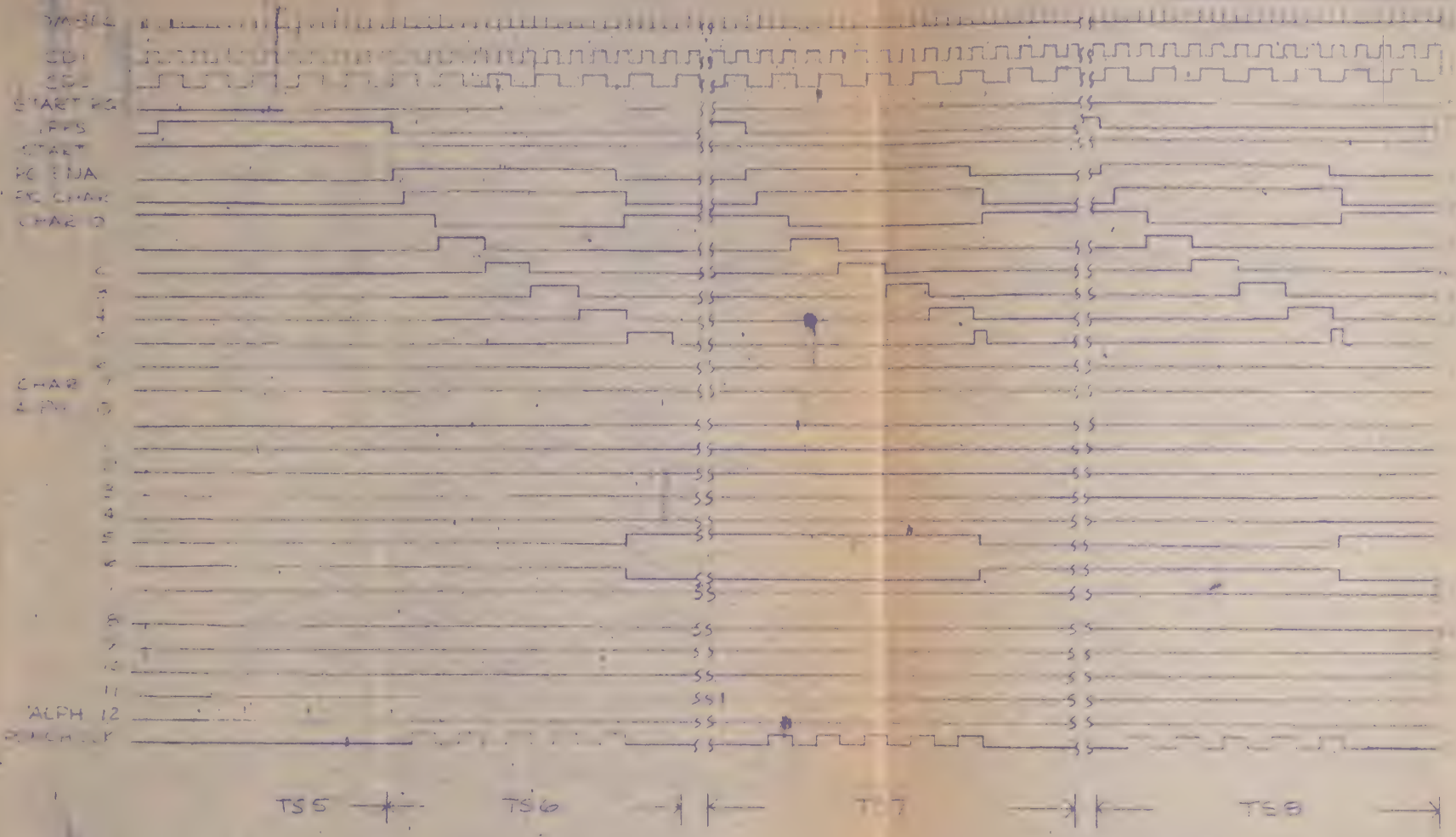
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

DWN		DES	
CHK		ENGR	
SCALE		P.N.	31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

SIZE	P 800442		REV
SHT 2 OF 4			

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .03
XXX ± .010
ANGLES ± 1/2°

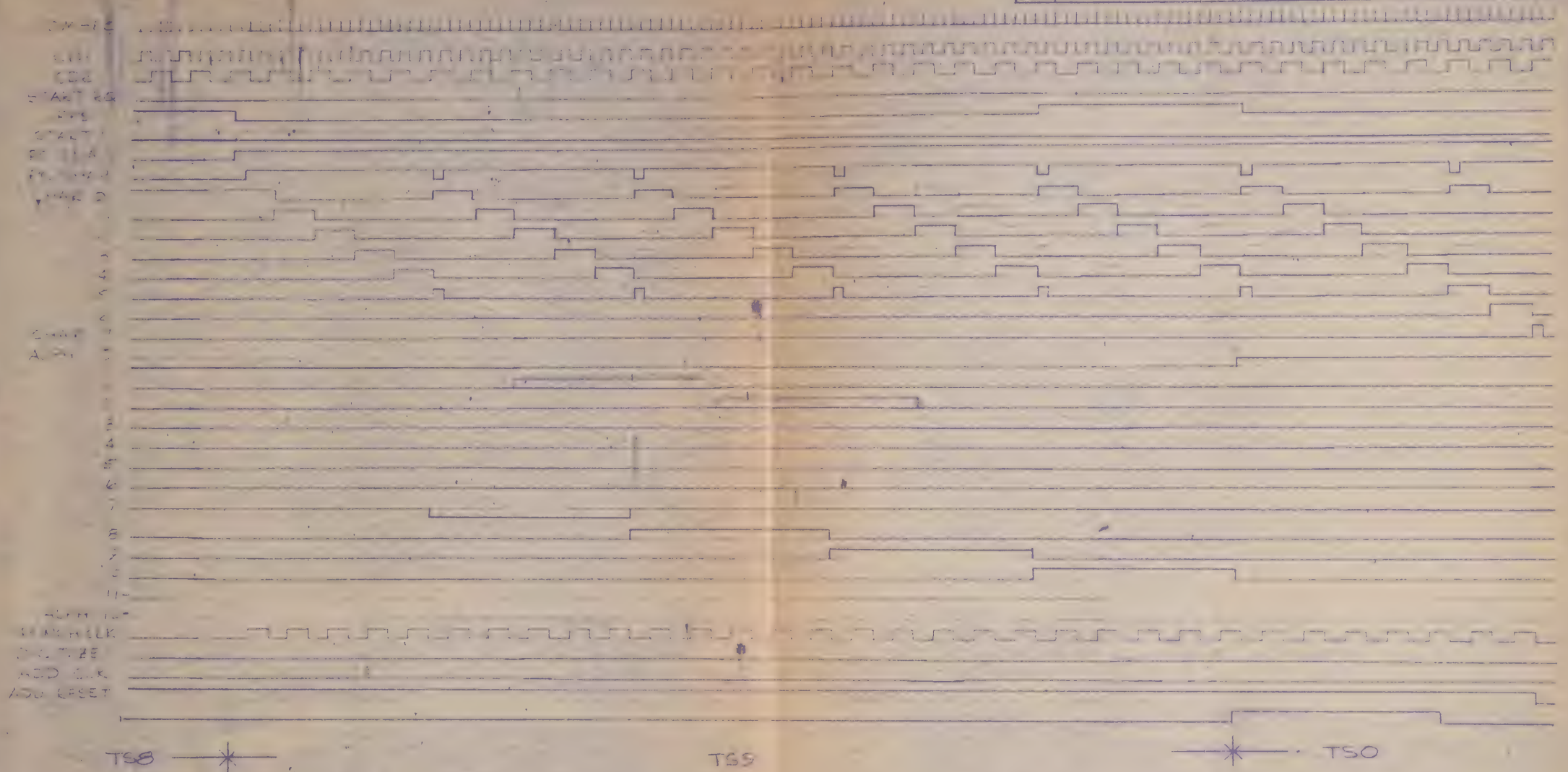
TITLE: TIMING DIAGRAM

DWN: [illegible] 4-24 | DES:
CHK: | ENGR:
SCALE: [illegible] | FSC: 31160

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B | 800442 | SIZE | SHT 3 OF 4 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL: .XX ±.03
.XXX ±.010
ANGLES ±1/2°

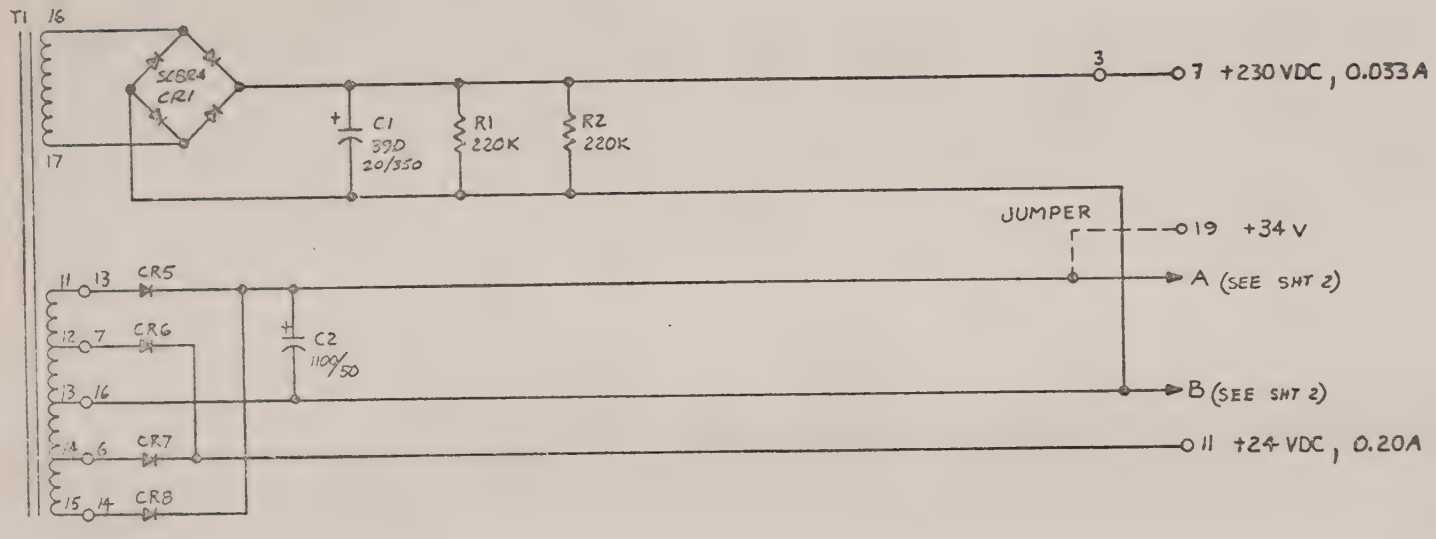
TITLE
TIMING DIAGRAM

DWN DES
CHK SNGR
SCALE FSC 31160

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B 800442

SIZE SHT 4 OF 4 REV



5. RESISTORS: 1/2W, CC, 10%.
4. DIODES: SCE2.
3. TRANSISTORS: NPN-2N3569; PNP-2N3645.
2. ALL CAPACITORS ARE IN μfd/VDC.
1. ALL RESISTORS ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

DRAFTSMAN	HGR	10/9/68
CHECKER		10/17/68
DESIGNER		10/17/68
ENGR	H.S.	10/17/68

NEXT ASSY

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

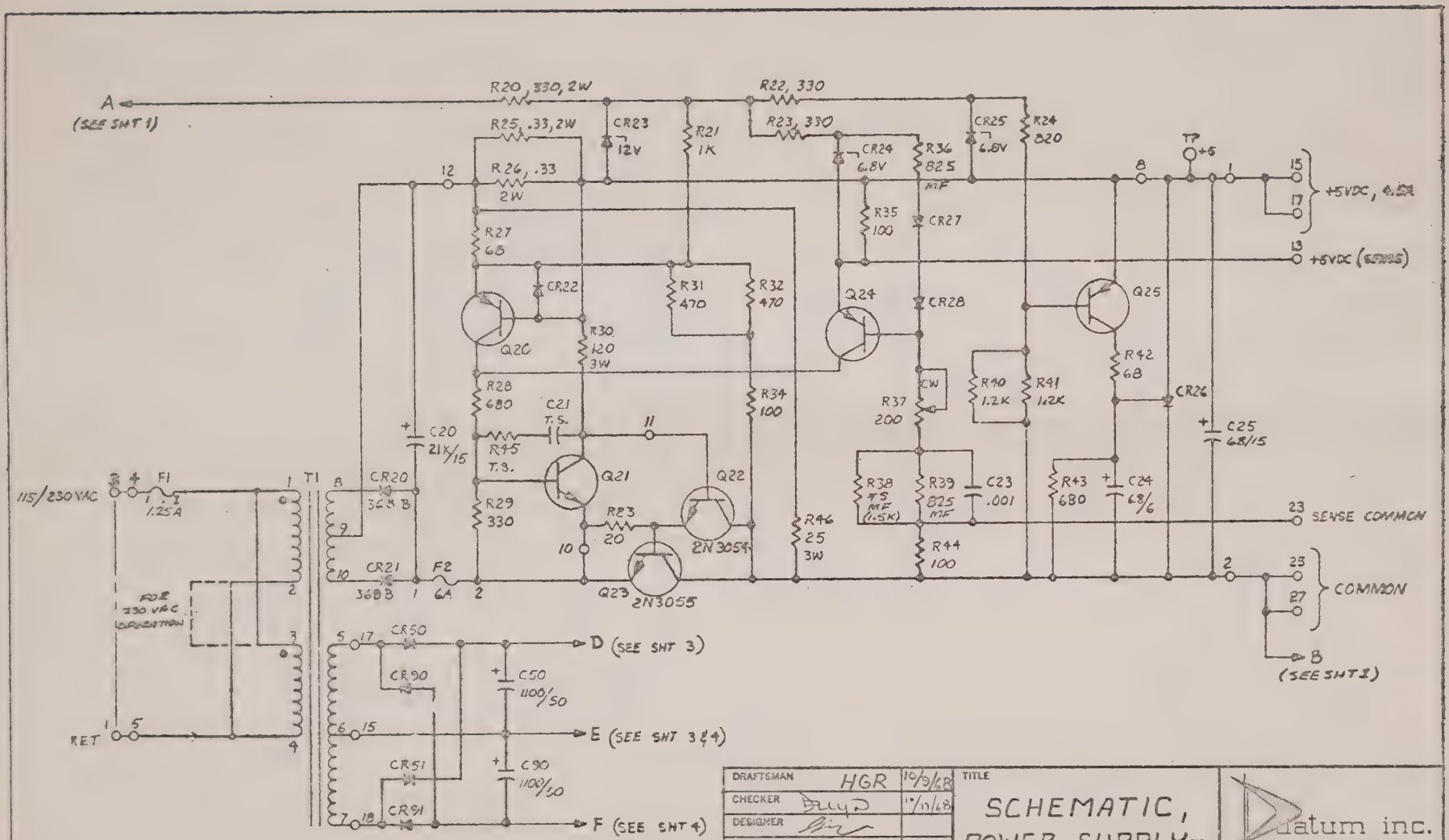
TITLE
SCHEMATIC, POWER SUPPLY-MULT OUTPUT

SCALE NONE

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIF.

B | 800015 | B

SIZE | SHT 1 OF 4 | REV



NOTES: SEE SHEET 1 OF 4

DRAFTSMAN	HGR	10/3/68
CHECKER		10/11/68
DESIGNER		
ENGR	K.S.	

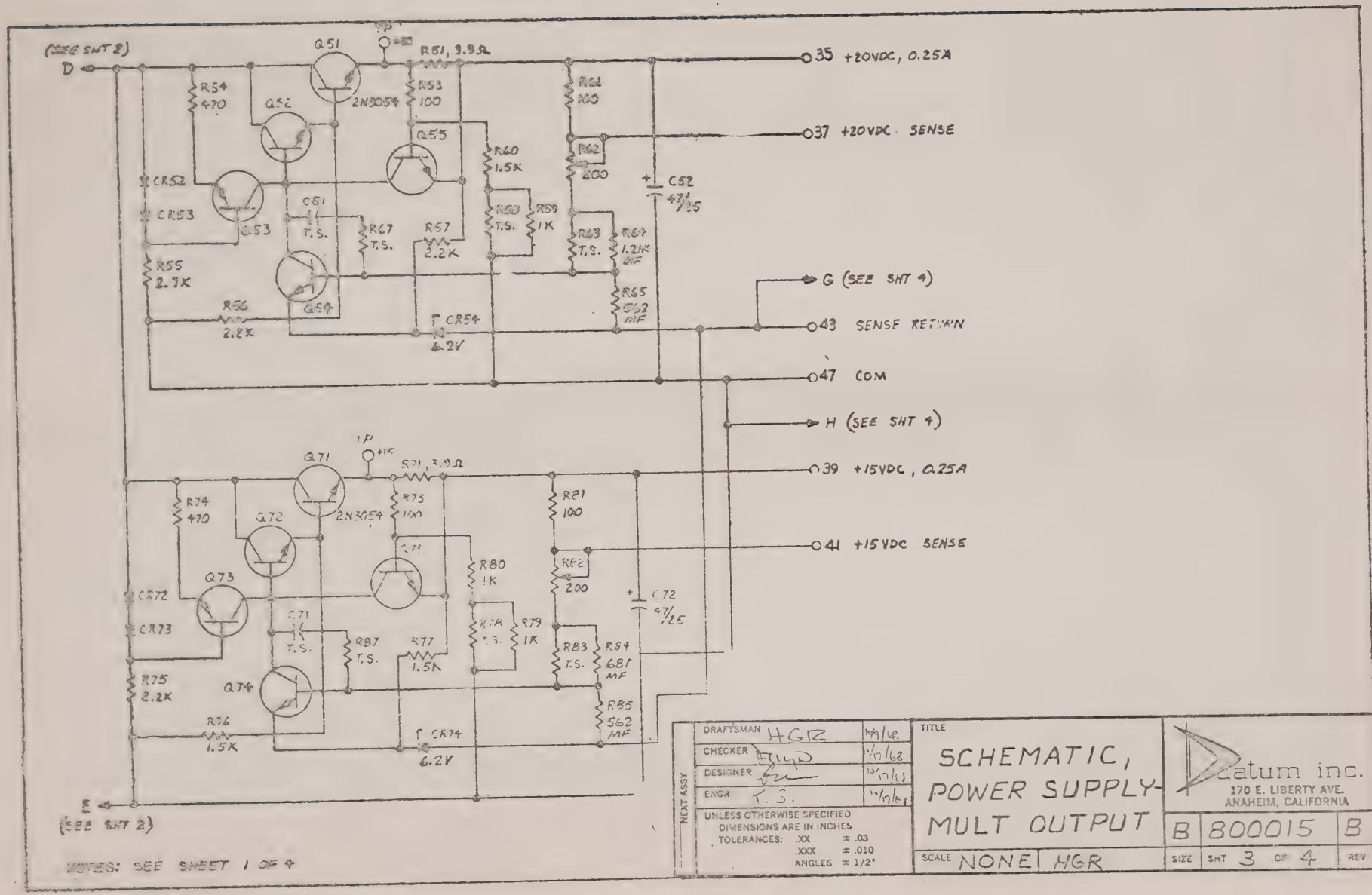
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03, .XXX ± .010, ANGLES ± 1/2°

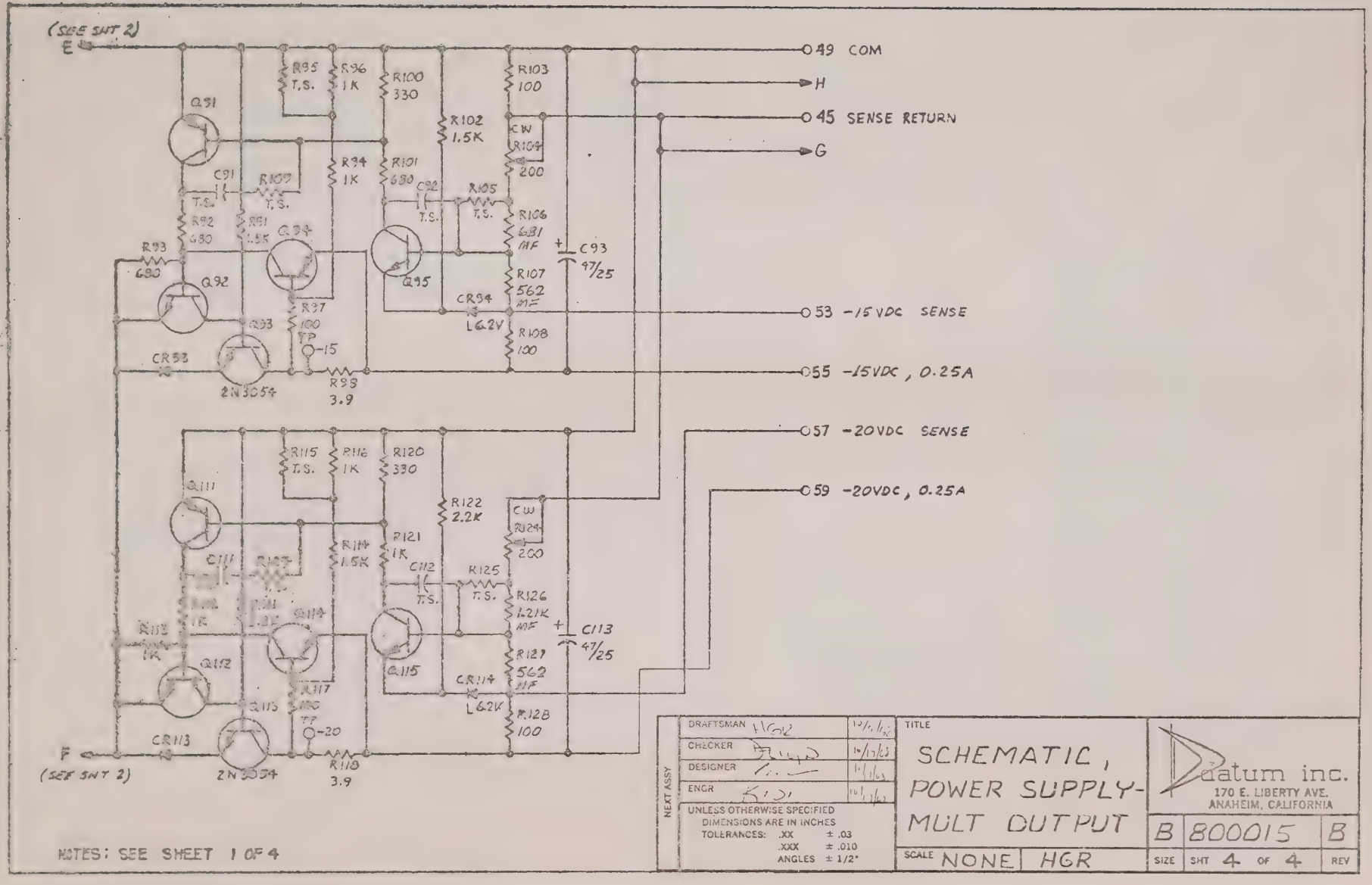
TITLE: SCHEMATIC, POWER SUPPLY-MULT OUTPUT

SCALE NONE

datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B	800015	B
SIZE	SHT 2 OF 4	REV


(SEE SHT 2)
D
Q51
2N3054
R51, 3.9Ω
R53 100
R54 470
Q52
Q53
Q54
Q55
R60 1.5K
R61 100
R62 200
C52 47/25
CR52
CR53
C51 T.S.
R57 2.2K
R59 1K
R63 T.S.
R64 1.21K MF
R65 562 MF
R55 2.7K
R56 2.2K
CR54 6.2V
35 +20VDC, 0.25A
37 +20VDC SENSE
G (SEE SHT 4)
43 SENSE RETURN
47 COM
H (SEE SHT 4)
39 +15VDC, 0.25A
41 +15VDC SENSE
Q71
2N3054
R71, 3.9Ω
R73 100
R74 470
Q72
Q73
Q74
R80 1K
R81 100
R82 200
C72 47/25
CR72
CR73
C71 T.S.
R77 1.5K
R79 1K
R83 T.S.
R84 681 MF
R85 562 MF
R75 2.2K
R76 1.5K
CR74 6.2V
E
(SEE SHT 2)
NOTES: SEE SHEET 1 OF 4
NEXT ASSY
DRAFTSMAN HGR 10/9/68
CHECKER 10/17/68
DESIGNER 10/17/68
ENGR K.S. 10/16/68
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03 .XXX ± .010
ANGLES ± 1/2°
TITLE
SCHEMATIC, POWER SUPPLY-MULT OUTPUT
SCALE NONE HGR
Datum inc.
170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA
B 800015 B
SIZE SHT 3 OF 4 REV



NOTES: SEE SHEET 1 OF 4

DRAFTSMAN	HGR	10/1/63
CHECKER		10/10/63
DESIGNER		10/1/63
ENGR		10/1/63

NEXT ASSY

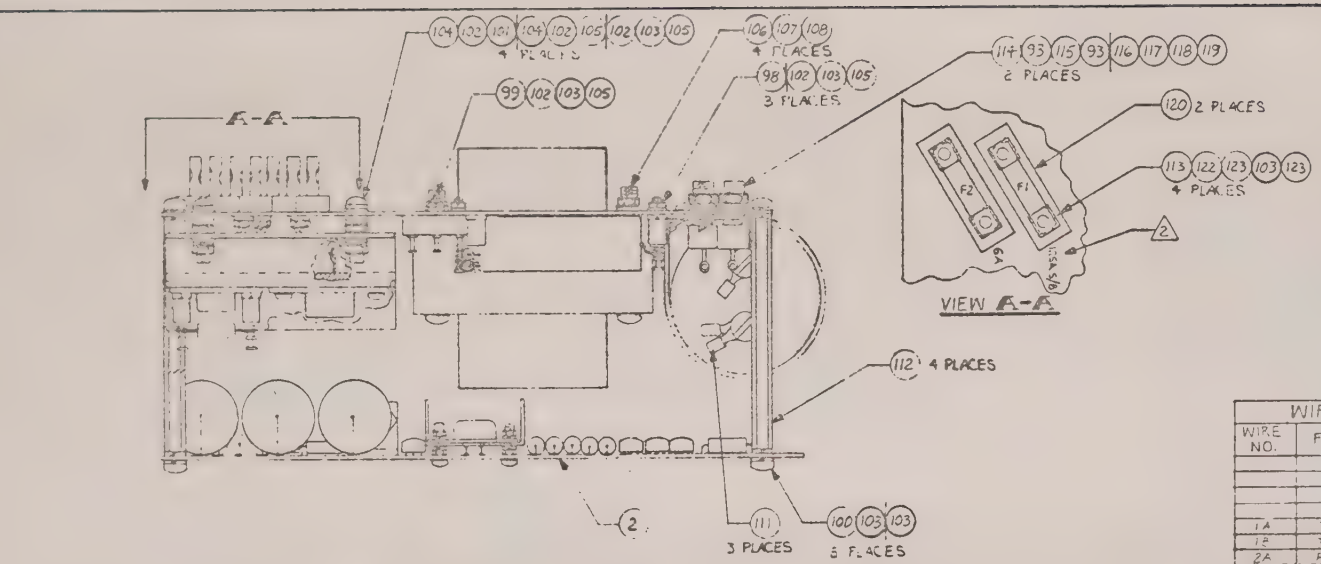
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .03, .XXX ± .010, ANGLES ± 1/2°

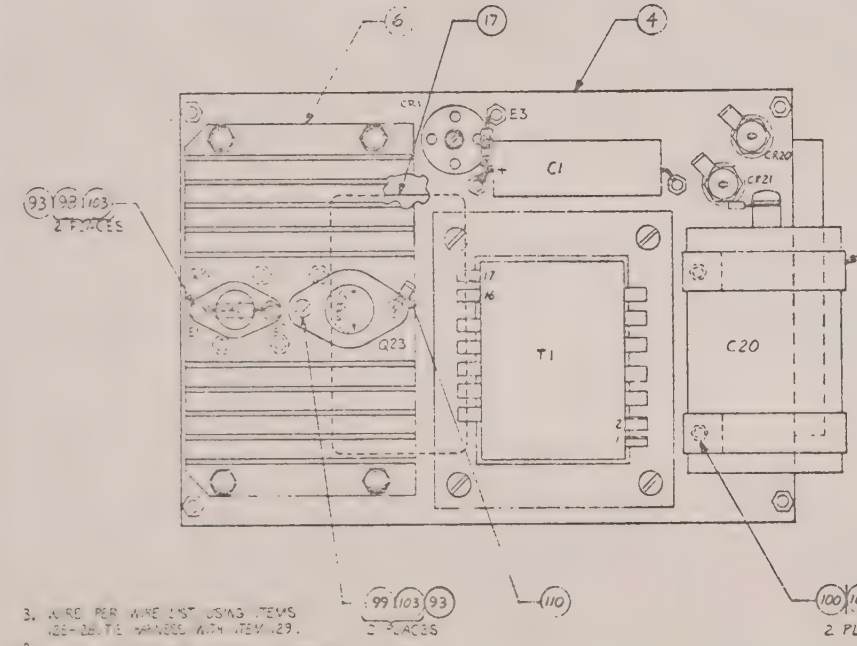
TITLE: SCHEMATIC, POWER SUPPLY-MULT OUTPUT

SCALE NONE HGR

Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

B	800015	B
SIZE	SHT 4 OF 4	REV





NAMEPLATE DATA
TITLE: POWER SUPPLY, AC/AC
PART NO: PS109
SERIAL NO: PER ATP
CUST CONT NO: 940001A
ORDER NO: PER SALES ORDER
DATE: MONTH - YEAR SHIPPED
INPUT: 105-130 VAC 50-400 HZ
OUTPUT: MULTIPLE, DC

WIRE LIST PS109

WIRE NO.	FROM	TO	WIRE SIZE
1A	T1-1	F-2	16
1B	T1-	T-3	
2A	F1-1	A1-4	
3A	T1-3	T1-4	
3B	T1-2	A1-5	
4A	T1-6	CR1-A2	
5A	T1-7	CR1-A1	
6A	CR1-NEG	E3	
6B	CR1-NEG	E2	
6C	C1-NEG	F2	22
6D	Q23-C	A1-9	18
6E	T1-13	A1-16	16
6F	Q23-C	CR24-C	20
7A	C1-POS	C21-POS	22
7B	CR1-POS	A1-3	18
8A	T1-11	A1-13	
9A	T1-12	A1-7	
10A	T1-14	A1-6	18
11A	T1-15	A1-12	22
	T1-8	CR23-C	—
	T1-9	C21-C	—
	F1-2	C21-POS	—
14A	E1	C20-POS	22
14B	C20-POS	A1-12	16
15A	CR20-A	CR21-A	16
15B	CR21-A	C20-NEG	16
15C	C20-NEG	F2-1	18
16A	F2-2	Q23-E	18
16B	Q23-E	A1-10	22
17A	Q23-B	Q22-E	22
18A	Q22-E	A1-11	22
19A	A1-8	A1-1	18
20A	T1-4	A1-15	22
21A	T1-5	A1-17	22
22A	T1-7	A1-18	22
66	E3	C1-NEG	22

3. WIRE PER WIRE LIST USING ITEMS 125-128 TIE HARNESS WITH ITEM 129.

⚠ INK STAMP WITH BLACK INK APPROX AS SHOWN.

1. CIRCUIT DESIGNATIONS ARE SHOWN FOR REF ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED

DRAFTSMAN	HGR	10/9/89
CHECKER		
DESIGNER		
ENGR		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: XX ± .03, XXX ± .010, ANGLES ± 1/2°

NEXT ASSY

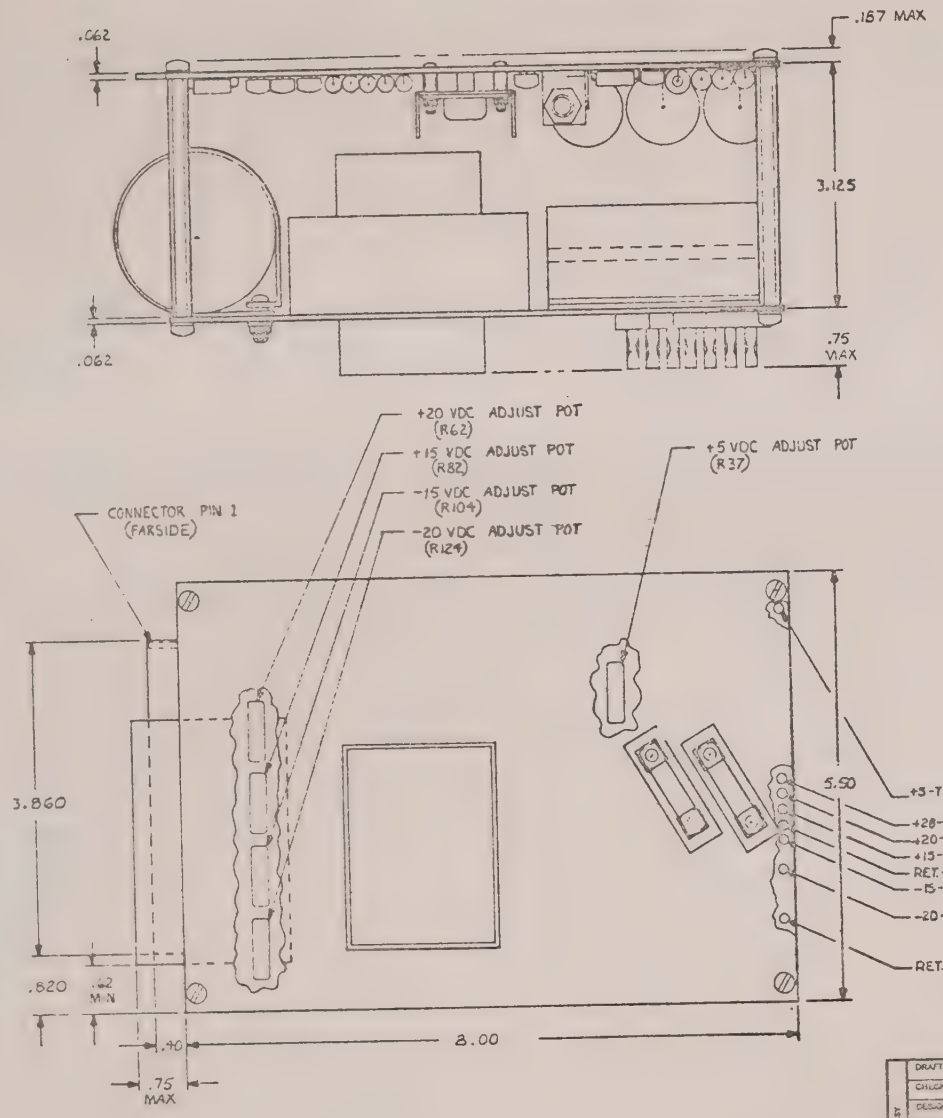
TITLE: POWER SUPPLY ASSY, AC/DC MULTIPLE OUTPUT

SCALE 1/1

Datum inc. 175 E. LIBERTY AVE. ANAHEIM, CALIFORNIA

C | 940001 | A

SIZE | SHT 1 OF 2 | REV



CONNECTOR CHART	
PIN NO.	FUNCTION
1	115 VAC
3	115 VAC
5	SPARE
7	+230V, 0.033A
9	SPARE
11	+24V, 0.2A (F.W.R.)
13	+5V SENSE
15	+5VDC, 4.5A
17	+5VDC, 4.5A
19	+34V DC (.2A)
21	
23	15V, 15V, +20V, +22V RUN AND SOLENOID SUPPLY
25	+5V, +24V, +28V, +230V
27	"DIGITAL COMMON"
29	
31	
33	
35	+20VDC, 0.25A
37	+20V SENSE
39	+15 VDC, 0.05A
41	+15V SENSE
43	±15V, ±20V
45	"ANALOG" SENSE RETURN
47	±15V, ±20V
49	"ANALOG" COMMON
51	SPARE
53	-15V SENSE
55	-15VDC, 0.05A
57	-20V SENSE
59	-20VDC, 0.25A
61	SPARE

DRAFTSMAN	HGR	9/5/78
CHECKER		
DESIGNER		
ENGR		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: XX ± .03, .XXX ± .010, ANGLES ± 1/2°

PLOT ASSY

TITLE
CONTROL DRAWING
POWER SUPPLY

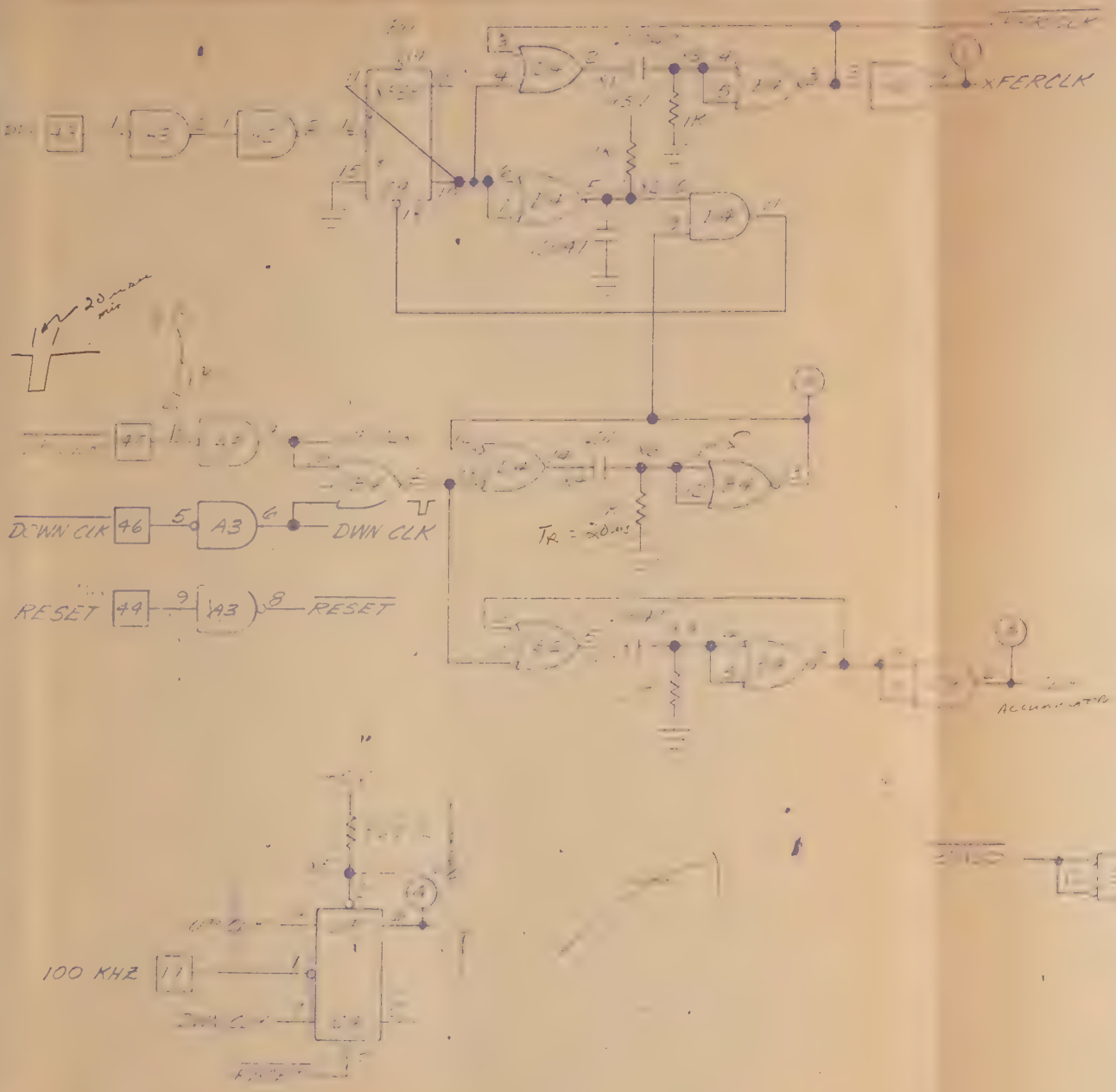
SCALE 1/1

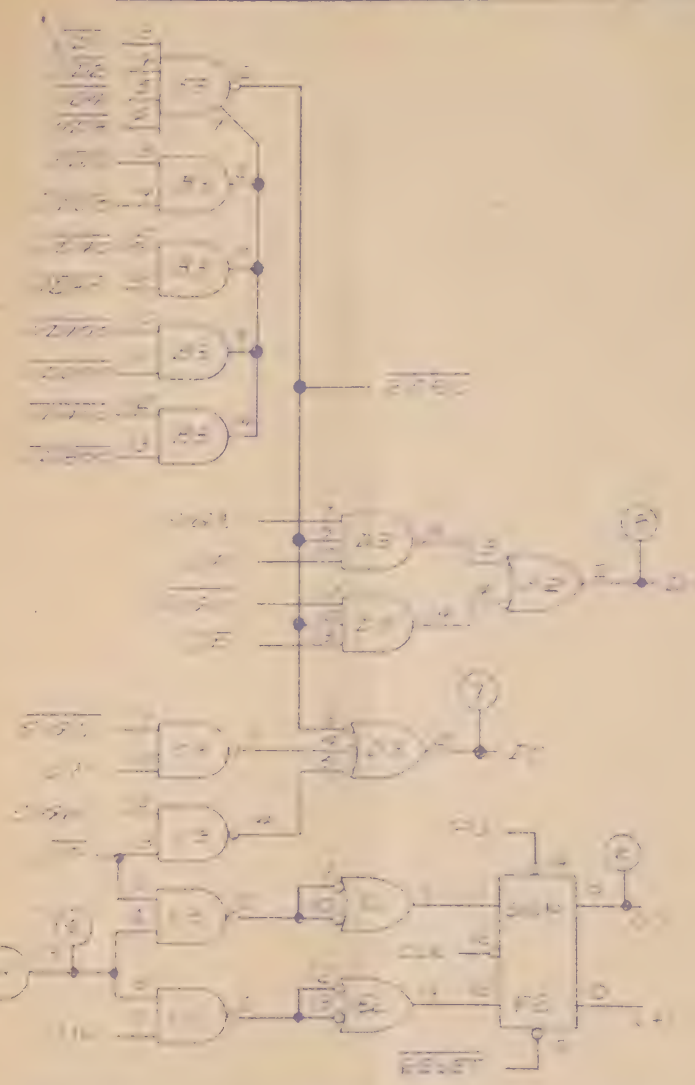
Datum inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

C | 340001 | A

SIZE | SHT 2 OF 2 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES · TOL: .XX ± .03 · .XXX ± .010 · ANGLES ± 1/2°

TITLE: UP DOWN COUNTER LOGIC

DWN TE 44	4/20/76	DES	
CHK		ENGR	
SCALE NONE		FSC 31160	

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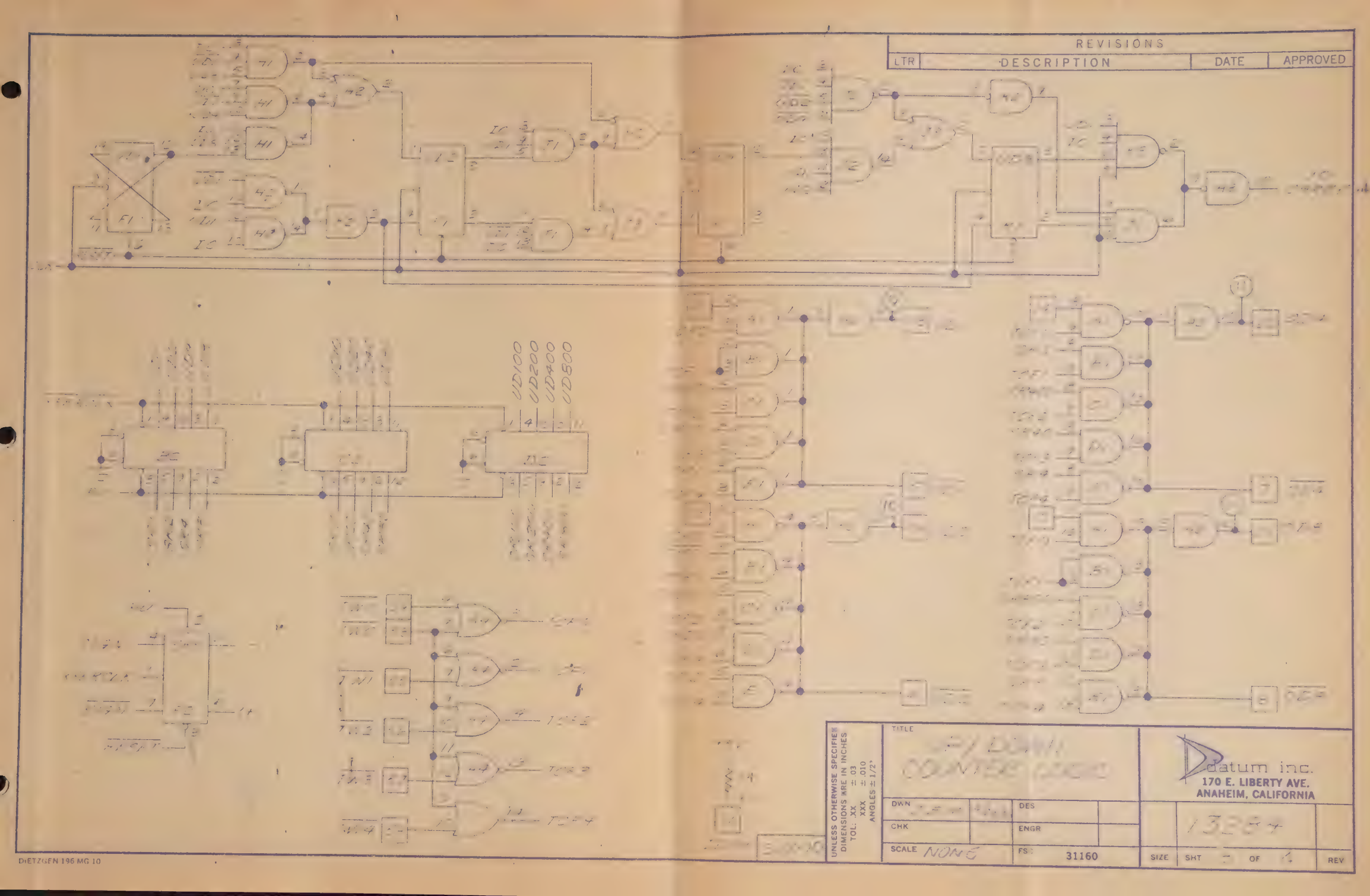
ANAHEIM, CALIFORNIA

1228-4

SIZE | SHT 2 OF 4 | REV

DIETZGEN 196 MG-10



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: U/D/W/ COUNTER (CMOS)

DWN		DES	
CHK		ENGR	
SCALE NONE		FS: 31160	

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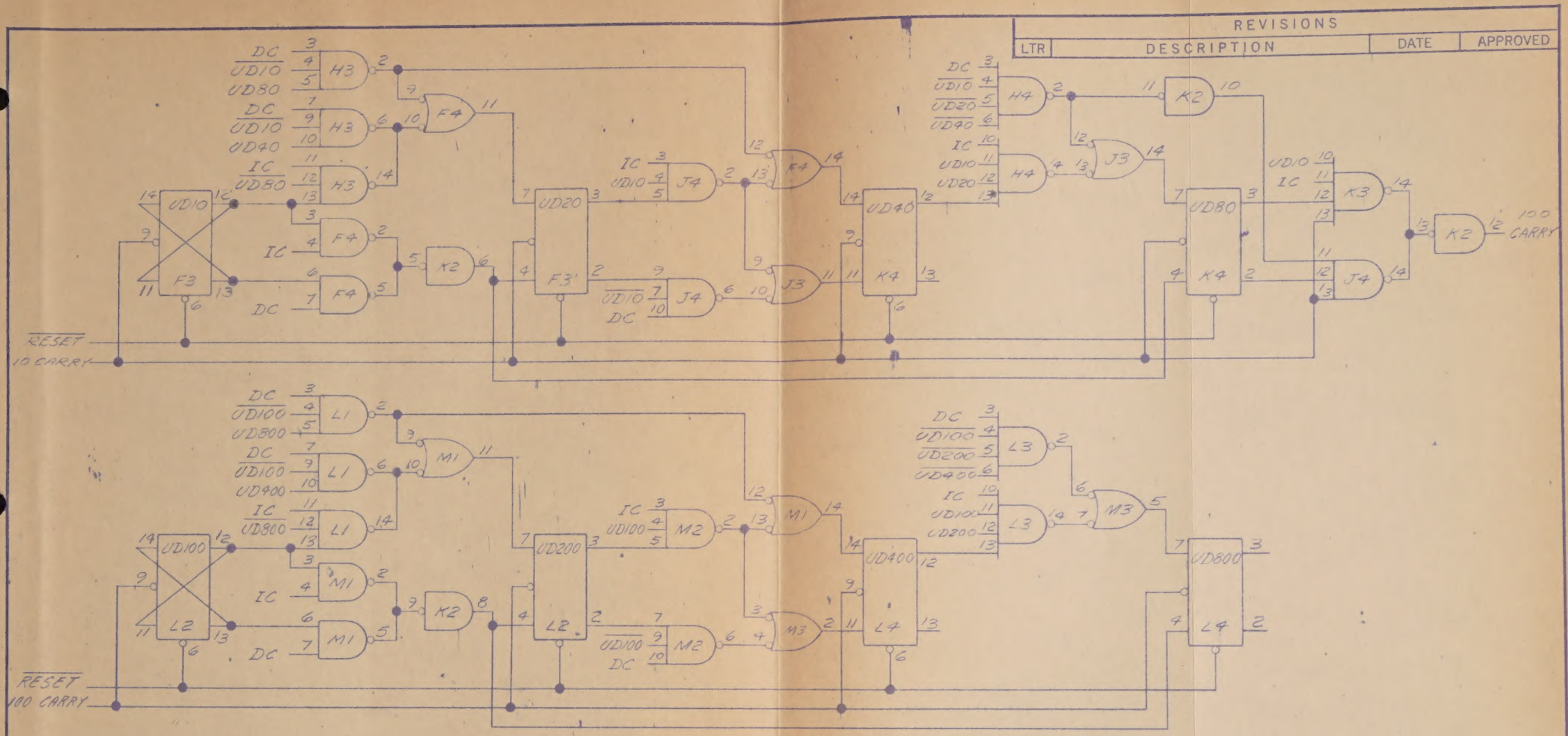
ANAHEIM, CALIFORNIA

13284

SIZE | SHT 2 OF 4 | REV

DIETZGEN 196 MG 10



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

5-22-70

TITLE: UP/DOWN COUNTER LOGIC

DWN J.E.M.	4/29/70	DES		
CHK		ENGR		
SCALE NONE		FSC 31160		

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SIZE | SHT 4 OF 4 | REV

DIETZGEN 196 MG-10

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